Gallium nitride transistors fabricated on cubic silicon carbide on silicon

Devices with gold-free ohmic contacts rival the fastest GaN HEMTs on silicon or silicon carbide with gold-based ohmic contacts, according to researchers in Germany.

Researchers in Germany have developed gallium nitride (GaN) high-electron-mobility transistors (HEMTs) on silicon carbide (SiC) layers on silicon wafers [Wael Jatal et al, IEEE Electron Device Letters, published online 11 December 2014]. The ohmic source-drain contacts were gold-free (Au-free) titanium nitride on titanium (TiN/Ti). The researchers came from Technische Universität Ilmenau and Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH (IMMS GmbH).

GaN-based HEMTs are being developed for radio frequency (RF) power amplification, based on high operating frequencies combined with high output power. The best GaN transistors are generally produced on hexagonal (4H) polytype SiC wafers, which are expensive and are of smaller diameter than is available with silicon.

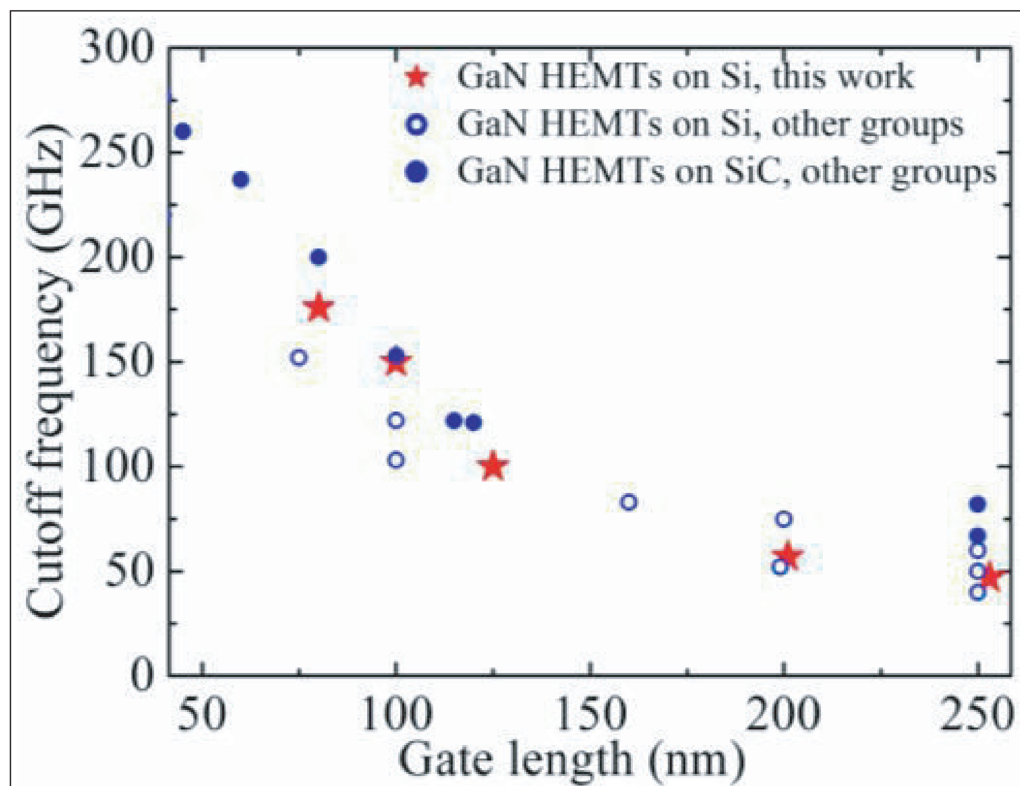

Figure 1. Comparison of cutoff frequencies of GaN HEMTs on silicon with barrier design A with best data reported by other groups for GaN HEMTs on silicon and on SiC.

The substrate used by Jatal et al was low-resistivity (3mΩ-cm) (111)Si on which 3C cubic polytype SiC had been deposited. The SiC growth began with 3nm carbonization with ethylene (C_2H_4) precursor. Further SiC was grown by adding silane (SH_4) as a silicon chemical vapor deposition (CVD) precursor.

Metal-organic chemical vapor deposition (MOCVD) was then used to apply 100nm aluminium nitride (AlN) as an interlayer, and GaN buffer. The barrier structure consisted of $Al_{0.2}Ga_{0.8}N$/AlN (design A) or $Al_{0.35}Ga_{0.65}N$ (design B). The AlGaN barrier thickness in both cases was 20nm. The AlN spacer between the AlGaN barrier and GaN buffer of design A was 2nm. The structures were capped with 2nm GaN.

The epitaxial design A achieved a Hall mobility of 1760cm^2/V-s, compared with 1200cm^2/V-s for design B. The sheet carrier densities were very similar at 7.5x10^{12}/cm^2 for design A and 7.2x10^{12}/cm^2 for design B.

The nickel-gold HEMT gate had two fingers of total width 150μm. The gate was centered in the 2μm source–drain gap.

The ohmic contacts for the source-drain regions were applied using magnetron sputtering of titanium. The initial deposition was 20nm titanium followed by 100nm titanium nitride. The titanium nitride was formed through reactive magnetron sputtering in argon/nitrogen atmosphere and annealing at 850°C in nitrogen.

Table 1. Results of DC and RF characterization of 100nm-gate HEMTs. DC measurements at 10V drain–source voltage (V_{DS}): maximum drain current (I_D) and peak transconductance (g_m). On-resistance (R_{on}) measured at low drain voltage with zero gate potential. Also shown are contact resistance (R_C), sheet resistance (R_S), specific contact resistance ρ_C), and cut-off frequencies (f_T) at 10V and 20V V_{DS} (−2.75V gate potential).

Barrier design	I_D	g_m	R_{on}	R_C	R_S	ρ_C	f_T at 10V	f_T at 20V
A	1.13A/mm	388mS/mm	0.9Ω-mm	0.13Ω-mm	169Ω/sq	1×10^{-6}Ω-cm^2	115GHz	150GHz
B	0.95A/mm	360mS/mm	1.6Ω-mm	0.6Ω-mm	365Ω/sq	1×10^{-5}Ω-cm^2	79GHz	107GHz

The specific contact resistance of Ti/TiN structures was ~10^{-6}Ω-cm^2. The contact resistance was 0.13Ω-mm. The root-mean-square (rms) roughness was 1.8nm. The researchers claim that their Ti/TiN structure is among the best gold-free structures so far.

The researchers comment: "We ascribe the low contact resistivity to the conversion of Ti into TiN causing the formation of nitrogen vacancies in the barrier layer which lead to a high doping level of the AlGaN underneath the contact."

The team carried out a number of characterizations on a 100nm-gate-length device (Table 1). The researchers attribute the improved performance of design A HEMTs to reduced alloy scattering due to the AlN spacer layer.

The RF measurements were carried out between 0.1GHz and 50GHz. Using extrapolations and de-embedding corrections, the cut-off frequency (f_T) for an 80nm-gate HEMT at 20V drain bias and −2.75V gate potential was estimated at 176GHz. The maximum oscillation frequency (f_{max}) was 70GHz. The low f_{max} was blamed on the simple rectangular gates and low-resistance substrate that was used. "Significant improvements of fmax can be expected by using mushroom gates with reduced gate resistance and high-resistivity substrates," the research team writes.

By contrast, the best 80nm-gate $Al_{0.35}Ga_{0.65}N$/GaN HEMTs demonstrated a poor f_T of only 115GHz at 20V drain voltage. HEMTs on SiC can achieve f_T values of 200GHz with a 75nm gate length. The corresponding value for HEMTs on silicon is 152GHz.

Comparing their results with those of others (Figure 1), the researchers comment: "It can be seen that our 80nm-gate HEMT shows competitive f_T performance compared to GaN HEMTs on Si (with Au-based and Au-free contacts) reported by other groups. Moreover, our GaN HEMTs on Si with barrier design A rival successfully the best reported GaN HEMTs on SiC substrates in the 80–125nm gate-length range." ■

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