Boosting speed & breakdown voltage performance of Schottky barrier diodes

Mike Cooke reports on recent developments with GaAs and III-nitride devices.

Schottky barrier diodes (SBDs) are often used in electronics circuits aiming to benefit from low turn-on voltages and high speed.

The fabrication of Schottky rather than pn diodes allows the turn-on voltage to be reduced significantly below that suggested by the bandgap energy. This particularly impacts gallium nitride (GaN) devices, since the large ~3V turn-on of pn diodes leads to large power losses in switching applications. However, Schottky diodes tend to have lower breakdown voltages and higher on-resistance than pn devices. Improving breakdown with thicker drift layers tends to increase on-resistance.

High speed arises from the domination of current flow by majority carriers so that switching does not have to wait for the recombination of electron and holes. However, as frequencies increase to the terahertz and submillimeter-wavelength level, fabrication becomes challenging due to the more restricted size of the device and high sensitivity to parasitic elements.

Here we look at recent research progress for GaAs (gallium arsenide) and GaN Schottky barrier diodes.

SU-8 bonding GaAs to silicon

The University of Virginia and Dominion MicroProbes Inc in the USA have reported the development of a submillimeter-wave radio frequency (RF) GaAs quasi-vertical SBD on silicon [Linli Xie et al, IEEE Electron Device Letters, 26 September 2017]. The III–V epitaxial material was transferred to the silicon using SU-8 photoresist as a bonding material. The team worked to eliminate problems with previous methods such as wafer fracture and delamination, which seriously impacted yields.

The researchers comment: "Diodes fabricated with the new process and measured in the 325–500GHz range using on-wafer RF probes exhibit low parasitic capacitance and series resistance, achieving device characteristics comparable to prior state-of-the-art submillimeter-wave diodes."

The team sees the integration of III–V materials on silicon as "an effective approach for realizing novel devices that combine outstanding RF characteristics

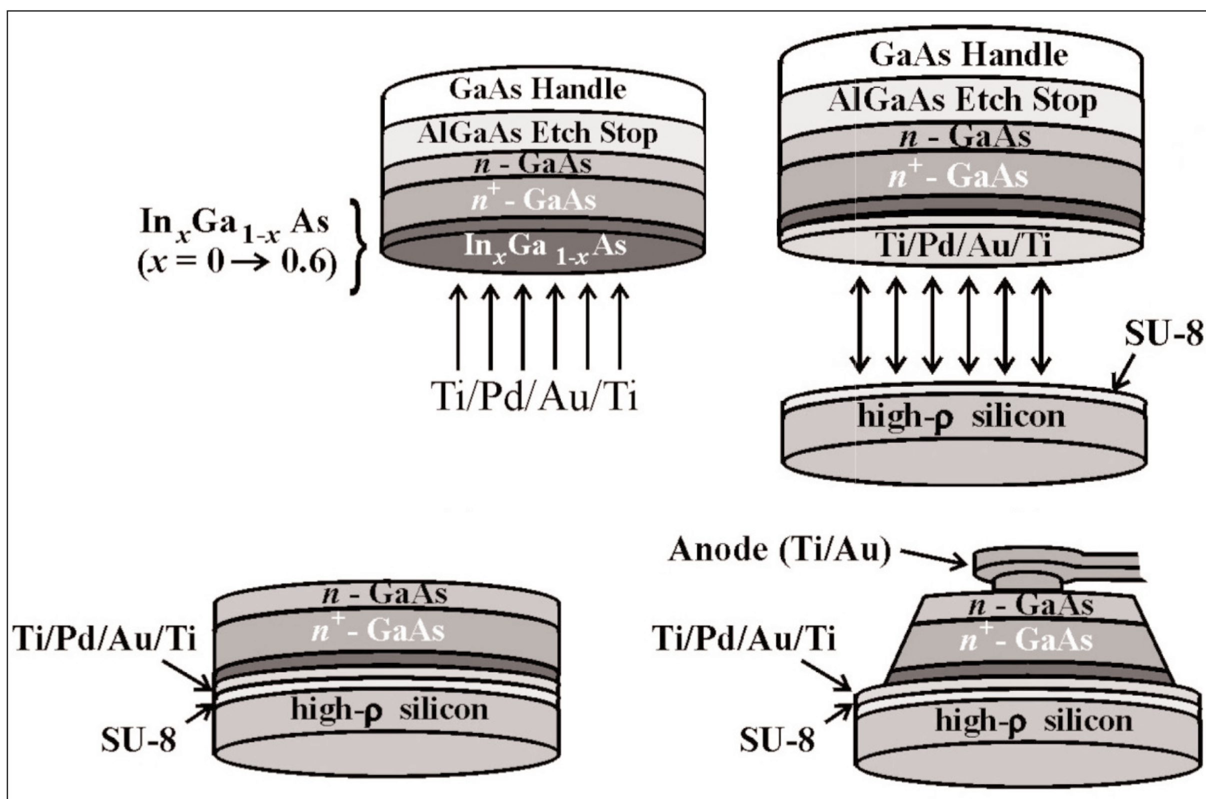


Figure 1. Quasi-vertical Schottky diode fabrication process: (a) Evaporation of Ti (20nm)/Pd (40nm)/Au (150nm)/Ti (20nm) ohmic contact. (b) Bonding of III-V epitaxial material to high-resistivity silicon. (c) Removal of GaAs handle and AlGaAs etch stop layers. (d) Etching of device mesa and formation of Schottky anode contact.

with a mechanically robust and low-loss substrate". They add: "Integration processes have been shown to provide flexibility in engineering new device geometries and can be exploited to mitigate the electrical parasitics and thermal grounding bottlenecks that frequently limit the performance of terahertz components."

The researchers have developed a process that builds on previous work (Figure 1). The III–V epitaxial structure on the 650μm-thick GaAs handle wafer consisted of 1μm aluminium gallium arsenide (AlGaAs) etch stop, 280nm n-GaAs, 1μm n^+-GaAs device, and highly doped indium gallium arsenide (InGaAs) cap layers. The cap ensured low-resistance ohmic contact with the titanium/palladium/gold/titanium (Ti/Pd/Au/Ti) metal stack. The cap consisted of 50nm graded-composition InGaAs and 40nm $In_{0.6}Ga_{0.4}As$.

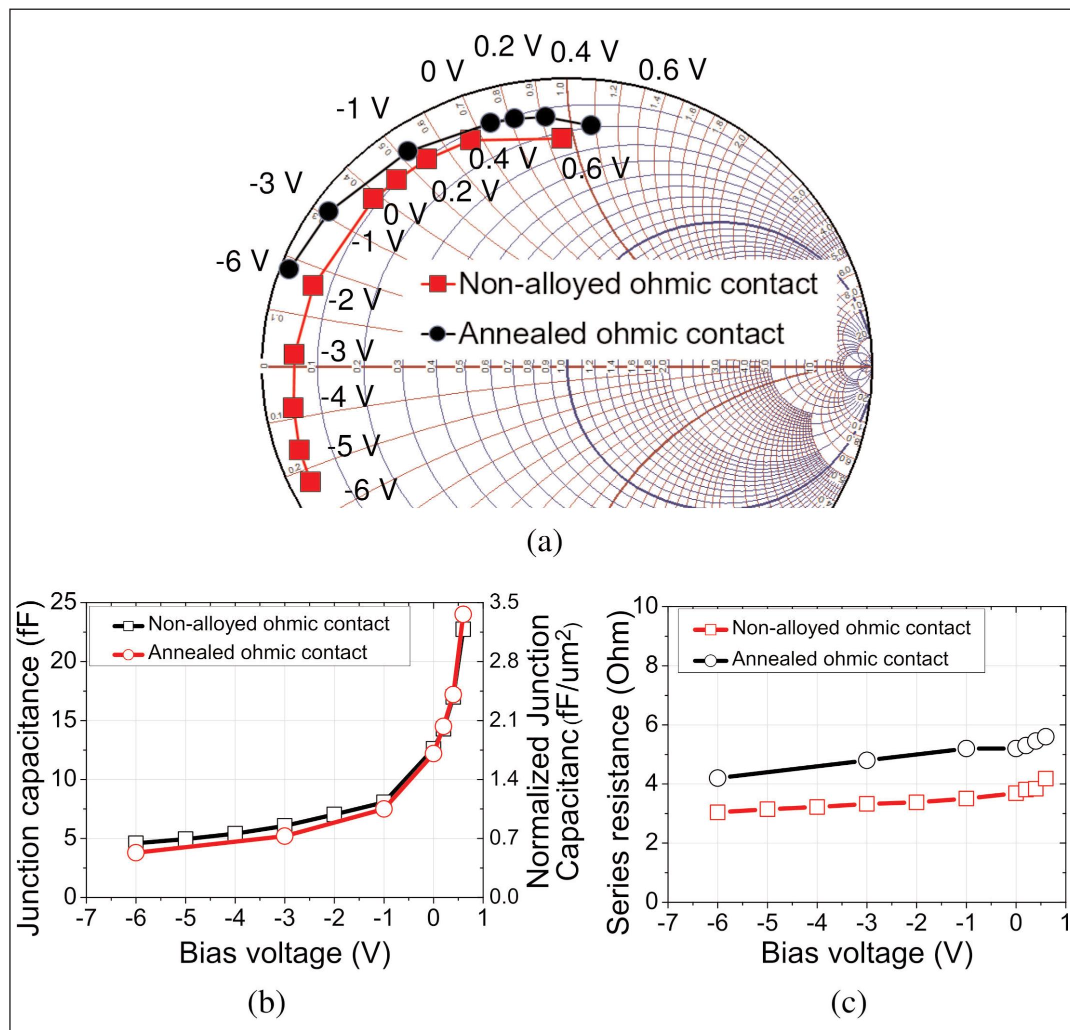


Figure 2. WR-2.2 on-wafer measurement results: (a) S_{11} versus voltage at 425GHz. (b) Extracted junction capacitance. (c) Extracted series resistance.

The unannealled metal layers were evaporated over the whole InGaAs surface and were not patterned. By not annealing the metal, a smooth surface was achieved that avoided wafer fracture as a result of the bonding with high-resistivity silicon, which has been a problem with the group's previous work.

The bonding material was 250nm-thick SU-8 negative epoxy-based photoresist, replacing the spin-on glass used previously. "The relatively low curing temperature of SU-8 (100–140ºC) compared to SOG (about 200ºC or higher), coupled with its relatively lower percent volume shrinkage after cross-linking, results in a more robust epitaxy transfer," the team comments. The low-temperature curing avoided the need for transparent substrates in ultraviolet curing contexts. The bonding involved spin-coating the SU-8, a 1-minute 110ºC soft-bake, an ultraviolet exposure, 40 minutes outgasing, and 40 minutes 140ºC curing.

The GaAs handle wafer was etched away by 50ºC etching in nitric acid and then citric acid solutions. The AlGaAs etch stop was removed by hydrochloric acid.

The diodes were fabricated by etching mesas down to the silicon with a combination of wet and dry etches: sulfuric acid and hydrogen peroxide in deionized water solution wet etch (GaAs); reactive ion etch (Ti, SU-8); sputter etch (Au); and wet chemical etch (Pd, Au). The GaAs mesa was further etched to give semiconductor material on a pedestal of exposed metal.

The further metalization of ohmic and air-bridge finger Schottky contacts, along with other circuit elements, were fabricated using standard techniques.

Direct-current measurements gave 1.19 ideality factor, 4.2Ω resistance, 0.1pA saturation current, 33.7mS/μm^2 normalized conductance, and 0.014pA/μm^2 normalized saturation current. Reverse-bias breakdown occurred at 9.5V.

High-frequency characterization was carried out for operation in the WR-2.2 rectangular waveguide (0.570mmx0.285mm, 325–500GHz) band (Figure 2). S-parameter characterization focused on the S_{11} reflection coefficient. The zero-bias junction capacitance normalized to the anode area was 1.78fF/μm^2. The normalized series conductance was 38.4mS/μm^2. The unannealed ohmic contacts were found to have 1Ω lower series resistance, compared with previous annealed devices.

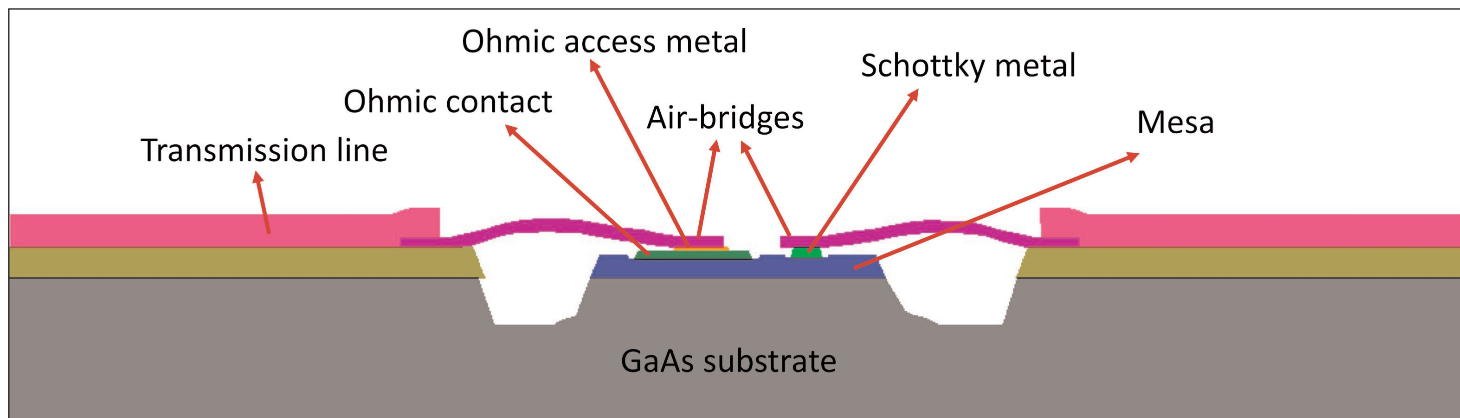


Figure 3. Schematic side view of fabricated diode.

Reducing costs

The University of Sherbrooke and École de Technologie Supérieure in Canada have developed a GaAs SBD fabrication technique aimed at low-cost submillimeter-wave performance [Sarvenaz Jenabi et al, Semicond. Sci. Technol., vol32, p105006, 2017]. The researchers used photolithography rather than the more expensive electron-beam patterning that is often used. Also, the number of metalization steps was reduced from five to two, reducing lithography alignment complexities from eight steps to five.

A significant reduction in parasitic capacitance was achieved by the use of air-bridge connections to the transmission lines (Figure 3). The researchers report: "The proposed fabrication method with large stand-off height for the air-bridge, wide and deep trenches has reduced the parasitic capacitance to less than 0.7fF. We expect a practical cut-off frequency of 0.85 and 1.4THz for these diodes."

The researchers used a GaAs wafer designed for heterojunction bipolar transistors (HBTs), etching away unwanted layers to leave a lightly doped n-GaAs layer for the Schottky contact and a heavily doped n-GaAs ohmic contact region. The ohmic contact layer was 350nm thick.

The multi-step metalization (multi-SM) used wet mesa etching, germanium/gold/nickel/gold ohmic contact evaporation, rapid thermal annealing (RTA), and titanium/gold Schottky contact evaporation. The height of the ohmic contact was raised to that of the Schottky contact by depositing titanium/gold.

Air-bridge formation began with titanium/gold evaporation and deep trench etching around the mesa. The trench was filled with resist that was etched back with oxygen plasma until the air-bridge contact features appeared. Further deposition and patterning formed the titanium/gold air-bridge wiring and transmission lines, where the resist materials were removed in the lift-off process.

The researchers simplified this process into a 'double-step' process by combining the Schottky contact, air-bridge and transmission line metalization into a single step. This needed the deep trench to be created before the Schottky metal deposition. Also, the trench filling material was changed so that it consisted of two resist types: a 'filling resist' and a 'cover resist'. The filling resist was chosen so that it was not affected by the cover resist developer. The filling resist also had a higher temperature tolerance.

The fill consisted of poly(methyl methacrylate) (PMMA) deposited in several layers. The lower part of the fill used low-concentration PMMA solution. The PMMA concentration was gradually increased for subsequent layers.

The thick cover resist was then spun onto the structure and patterned so that, after development, the cover resist was only found over the trench. The oxygen plasma etch rate for the cover resist was less than that of the PMMA so the final structure made an arch shape of resist over the trench. The non-trench surfaces were free of resist.

The researchers comment: "Unlike the multi-SM, this process is much less sensitive on the etching stop point, since another resist will be spun over to form and support the air bridges and T-shaped anode."

The T-shaped anode and air-bridge wiring was patterned through deep-ultraviolet lithography on a three-layer resist for metal lift-off processing. The bottom layer was poly-methyl-glutar-imide (PMGI). The top layer was from Shipley. The middle 'undercut' layer was chosen so that its developer would not affect the bottom PMGI layer. The PMGI layer enabled the formation of the tall-neck T-shaped anode. The titanium/gold metal was deposited after cleaning and passivation. The lift-off process then gives the Schottky contact (anode), air bridges, and transmission-line circuitry.

The capacitance of diodes with 1.5μm- and 1μm-diameter anodes were extracted as 7.1fF and 3.3fF, respectively. These values were based on S-parameter measurements between 2GHz and 40GHz. DC measurements (Figure 4) gave 5×10^{-16}A saturation current, 1.13 ideality, 0.817eV Schottky barrier height, and 34Ω diode resistance between 8mA and 10mA high current.

The diode was in the middle of a co-planar waveguide

(CPW) structure. The team reports: "The measurement results are valid for diodes fabricated by using both presented fabrication process since a single design was used in both processes."

Aluminium nitride SBDs with 1kV+ breakdown

Arizona State University (ASU) in the USA have claimed the first demonstration of 1kV-class aluminium nitride (AlN) SBDs [Houqiang Fu et al, IEEE Electron Device Letters, 5 July 2017] and record low turn-on voltage, less than 0.6V, for its latest vertical GaN-on-GaN SBDs [Houqiang Fu et al, Appl. Phys. Lett., vol111, p152102, 2017].

AlN has an ultra-wide bandgap of 6.2eV. Wide bandgaps are associated with the large critical fields (12.5MV/cm in AlN) that are needed in compact power handling devices. Other semiconductor materials used in or proposed for power devices have narrower bandgaps: 3.3eV for silicon carbide, 3.4eV for GaN, 4.8eV for beta-gallium oxide, and 5.5eV for diamond. AlN also has a large thermal conductivity of 340W/mK, which is also an attractive feature for power applications.

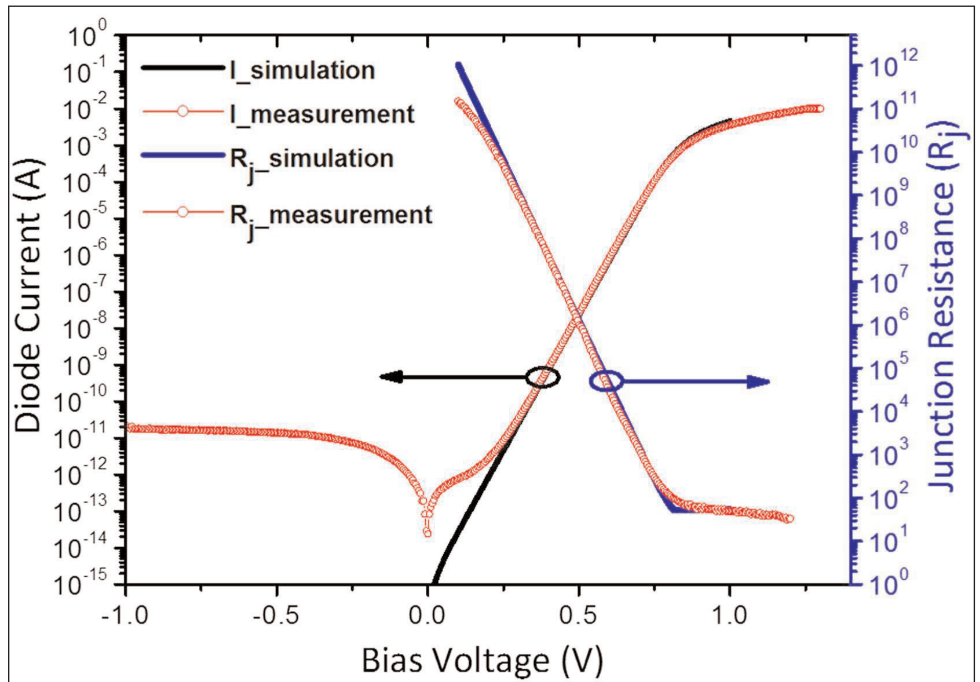


Figure 4. Simulated and measured current versus voltage bias of diode (left axis), and junction resistance versus voltage bias (right axis) for 1.5μm anode radius.

AlN's advantages have not led so far to commercial devices since there are material and fabrication challenges.

ASU's AlN material was grown by metal-organic chemical vapor deposition (MOCVD) on single-side-polished (0001) sapphire substrate off-cut 0.2º. The SBD structure (Figure 5) included 1μm unintentionally doped (UID) AlN underlayer (UL), 300nm silicon-doped n-AlN, and 2nm UID GaN cap.

According to the researchers, the device structure mimics silicon-on-insulator (SOI) technology, with a thin n-AlN epilayer active region on the thick resistive AlN underlayer. The purpose of the cap was to protect the underlying layers from oxidation, which can negatively impact device performance.

The researchers report that the AlN material demonstrated among the narrowest reported full-width at half maximum (FWHM) x-ray peaks for MOCVD AlN on sapphire — 46.8arcsec for the (0002) rocking curve and 159.1arcsec for (20$\bar{2}$4). These figures suggest dislocation densities of the order 10^8/cm^2.

The SBD was fabricated with 20nm/100nm/20nm/50nm Ti/Al/Ti/Au ohmic and 30nm/120nm platinum/gold (Pt/Au) Schottky contacts. The ohmic metal was patterned as a 400μm-diameter circular disk.

Two types of Schottky contact were made: a 100μm-diameter circular disk and 100μm-side square. The distance between contacts was 200μm. Surface passivation consisted of 200nm plasma-enhanced CVD silicon dioxide (SiO_2). There was no edge termination structure.

The ~10^5 on-off ratio of the devices is described by the team as being comparable to AlN devices on AlN substrates. The turn-on voltage of 1.2V (1.1V for square contacts) is smaller than previously reported values (more than 2V), according to ASU.

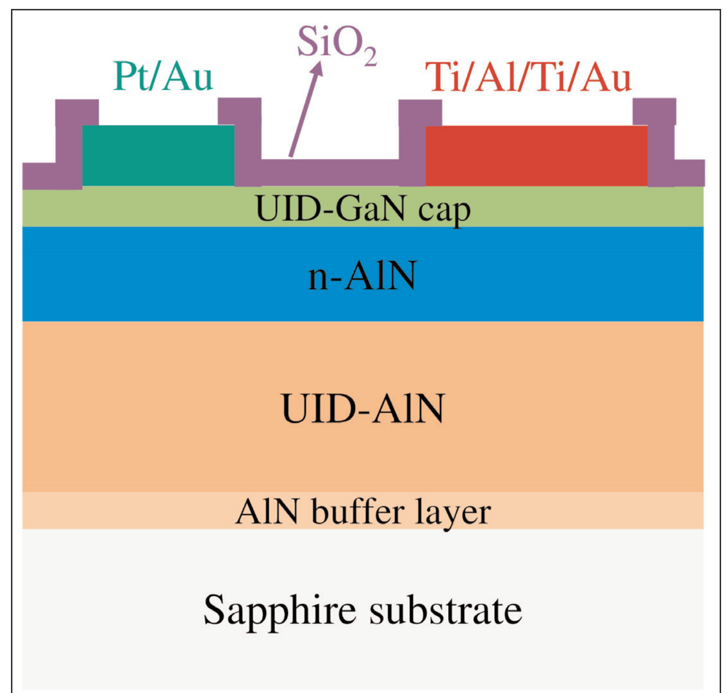


Figure 5. Schematic view of fabricated AlN SBDs on sapphire by MOCVD. Ohmic and Schottky contacts are in red and green, respectively.

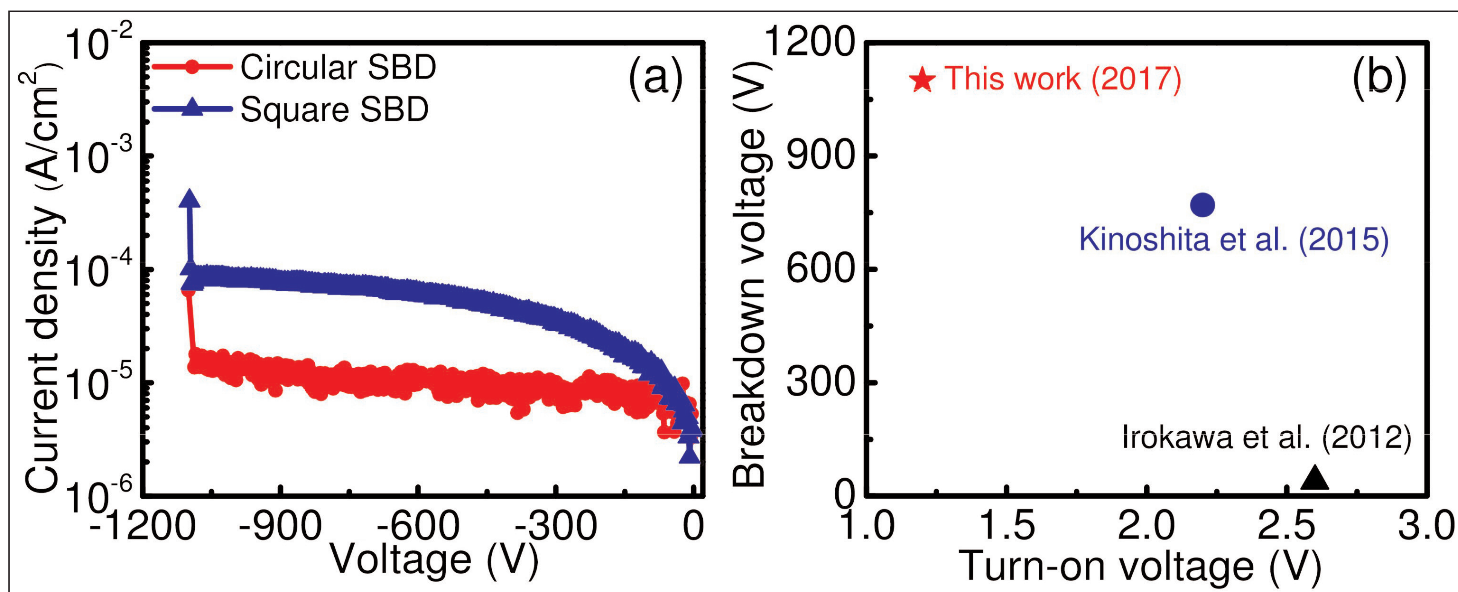


Figure 6. (a) Reverse current–voltage characteristics of circular and square AlN SBDs. (b) Comparison of breakdown and turn-on voltages of reported AlN SBDs.

The temperature dependence of the device performance suggests that the forward current was limited by thermionic emission. Schottky barrier height increased from 0.9eV to 1.6eV between 20ºC (room temperature — RT) and 200ºC. At the same time, ideality decreased from 5.5 (5.3 for square contact) to 2.2. Previous reported idealities of AlN SBDs have been greater than 8.

The researchers attribute the ideality behavior to "lateral inhomogeneity of the Schottky barrier interface". They add: "Note that the RT ideality factors (n = 5.5 and 5.3 for circular and square SBDs, respectively) obtained in this work were 2~3 times smaller than previous results, possibly due to improved material quality and metal/semiconductor interface."

Under reverse bias, the SBDs broke down only after 1kV, beating previous reports of ~700V for devices produced on free-standing AlN substrate by Japan- and US-based researchers (Figure 6). The ASU devices showed catastrophic damage at the edge of the Schottky contacts that was attributed to edge electric field crowding.

The team comments: "Improvement in the breakdown capability of the devices can be further expected by employing field-plate and/or edge termination. In addition, improving the material quality of n-AlN, increasing the resistivity of the UID AlN UL by Fe or C doping and optimizing the passivation strategies can also help to increase the breakdown voltage of the devices."

Reverse-bias leakage was generally less than 1nA.

GaN single and double drift layers

The ASU researchers also developed a double drift layer to increase the breakdown voltage in GaN-on-GaN SBDs.

Vertical devices have recently been developed on free-standing or bulk GaN substrates for power applications. The use of free-standing/bulk substrates avoids generating high threading dislocation densities (more than 10^9/cm^2 on sapphire) that provide unwanted leakage paths, reducing breakdown voltages.

The researchers used n^+-GaN bulk substrates from Sumitomo Electric Industries Ltd for MOCVD of the SBD materials (Figure 7). A conventional single-drift-layer diode, A, was compared with a double-drift-layer structure, B. Simulations suggested that diode B should be able to support much higher reverse biasing for the same peak electric field at the metal/semiconductor interface.

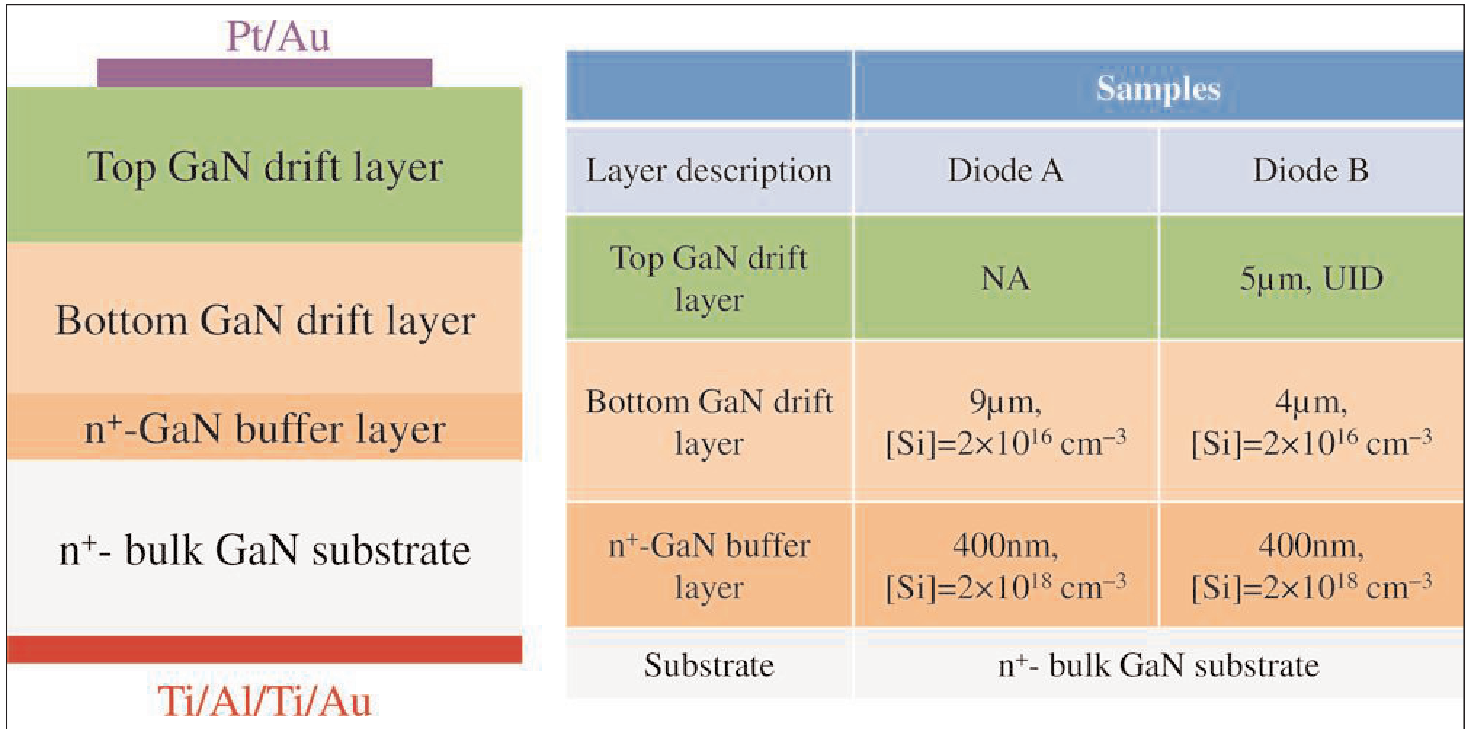
Using x-ray analysis the researchers estimated that the dislocation densities were in the low 10^6/cm^2 range in both samples - "significantly lower than that of typical GaN devices grown on sapphire (>10^9/cm^2)," they add.

Fabrication involved cleaning, inductively coupled plasma mesa etch, and the deposition of Schottky Pt/Au and ohmic Ti/Al/Ti/Au ohmic contacts. There was no passivation, field plate (FP) or edge termination.

The turn-on voltages were 0.52V and 0.59V for diodes A and B, respectively. This gave corresponding forward voltages for 0.1mA current flow of 1.0V and 1.2V. The turn-on voltages are described as record lows for vertical GaN-on-GaN diodes. The diode B had an ideality of 1.04, compared with 1.06 for diode A. These values are described as nearly ideal (i.e. unity factor) for GaN SBDs.

The off-current density, the measurement of which was hampered by the 0.1nA lower limit of the test equipment, was below 10^{-7}A/cm^2 for both diodes. The on/off current ratio was about 10^{10}, "among the highest values demonstrated in vertical GaN power diodes," says the team.

The on-resistance at 0.1A current was 1.39mΩ-cm^2 for diode A and 1.65mΩ-cm^2 for B. The slightly higher on-resistance of diode B is attributed to a lack of electrons in the top undoped drift layer. Subtracting out the effect of the substrate, the researchers estimate the drift-layer mobility to be 886.1cm^2/V-s and 1045.2cm^2/V-s



	Samples	
Layer description	Diode A	Diode B
Top GaN drift layer	NA	5μm, UID
Bottom GaN drift layer	9μm, $[Si]=2\times10^{16}$ cm^{-3}	4μm, $[Si]=2\times10^{16}$ cm^{-3}
n^+-GaN buffer layer	400nm, $[Si]=2\times10^{18}$ cm^{-3}	400nm, $[Si]=2\times10^{18}$ cm^{-3}
Substrate	n^+- bulk GaN substrate	

Figure 7. Cross section of GaN SBDs (left) and detailed descriptions of layers (right) for diode A and diode B.

for diodes A and B, respectively. The team comments: "Diode A had a lower electron mobility possibly due to stronger impurity scattering from silicon dopants."

The reverse-bias breakdowns for diodes A and B were, respectively, 340V and 503V (Figure 8). These values gave critical fields (1.17MV/cm and 1.30MV/cm, respectively) that were somewhat lower than the expected values based on the critical field of GaN (~3.0MV/cm). The team reports: "Since we did not employ FP or edge termination, the breakdown was expected to be determined by the device edge breakdown. Optical microscopy examination confirmed that the catastrophic damages of the GaN SBDs indeed occurred at the edge of Schottky contacts possibly due to severe edge electric field crowding."

Varying the temperature allowed extraction of the Schottky barrier heights (Φ_B): 0.69eV for diode A and 0.70eV for B. The team comments; "The low Φ_B values are partly responsible for the obtained record-low V_{ON} in forward bias. The measured Φ_B values are less than the theoretical values, which demands further investigations. Possible explanations include surface roughness, non-uniform current distribution, and so on." ■

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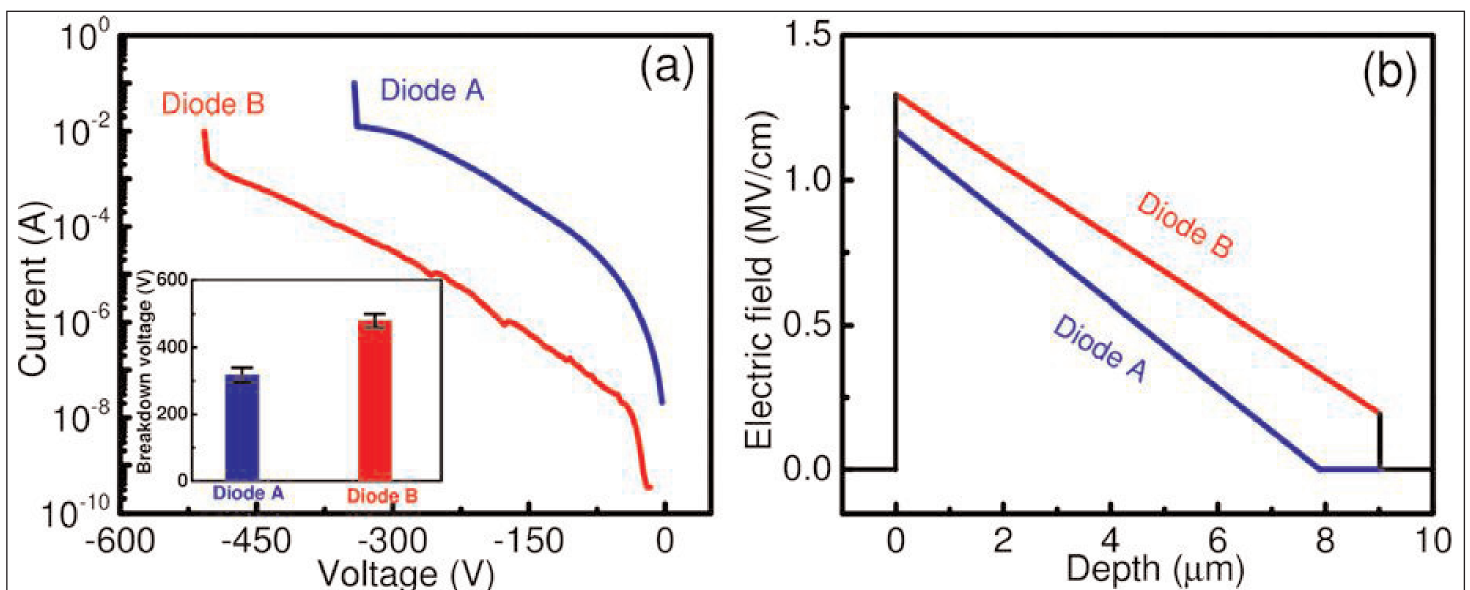

Figure 8. Reverse current–voltage characteristics of diodes A and B. Inset: measured breakdown voltages. (b) Electric field profiles along vertical direction of diodes.