InGaAs-on-insulator transistors with buried yttrium oxide

A simple MOS back-gate stack has been used to demonstrate what is claimed to be the first InGaAs-on-insulator transistor with a buried yttrium oxide layer, achieving effective mobility of 2000cm^2/V-s.

Korea Institute of Science and Technology has presented what it says is the first demonstration of indium gallium arsenide on-insulator ($In_{0.53}Ga_{0.47}As$-OI) transistors with a buried yttrium oxide (Y_2O_3 BOX) layer [SangHyeon Kim et al, IEEE Electron Device Letters, published online 31 March 2015].

The researchers see InGaAs-OI as a promising alternative to more complicated tri-gate devices. The use of Y_2O_3 should enable reduced equivalent oxide thickness (EOT) compared with aluminium oxide, on the basis of a higher dielectric constant (16 versus 9–12). Reduced EOT brings the gate effectively closer to the channel, improving electrostatic control.

A simple metal-oxide-semiconductor (MOS) back-gate stack transistor was constructed by layer transfer of InGaAs from its indium phosphide (InP) growth substrate to silicon with a Y_2O_3 buried layer (Figure 1). The InGaAs surface was prepared by native oxide removal and passivation with acetone, ammonium hydroxide, ammonium sulfide solutions. The clean surface was covered with 10nm of Y_2O_3 produced through electron-beam evaporation. The silicon target substrate was also covered with 10nm Y_2O_3, after cleaning with hydrofluoric acid.

The wafer bonding was achieved with hand pressure in air. The InP growth substrate and an InGaAs sacrificial layer were removed with hydrochloric and phosphoric acid wet etching. Nickel/gold was used for the source and drain electrodes. An InP etch-stop layer was selectively removed from the source and drain areas, but left in place over the channel region to reduce surface effects, which can impact effective mobility.

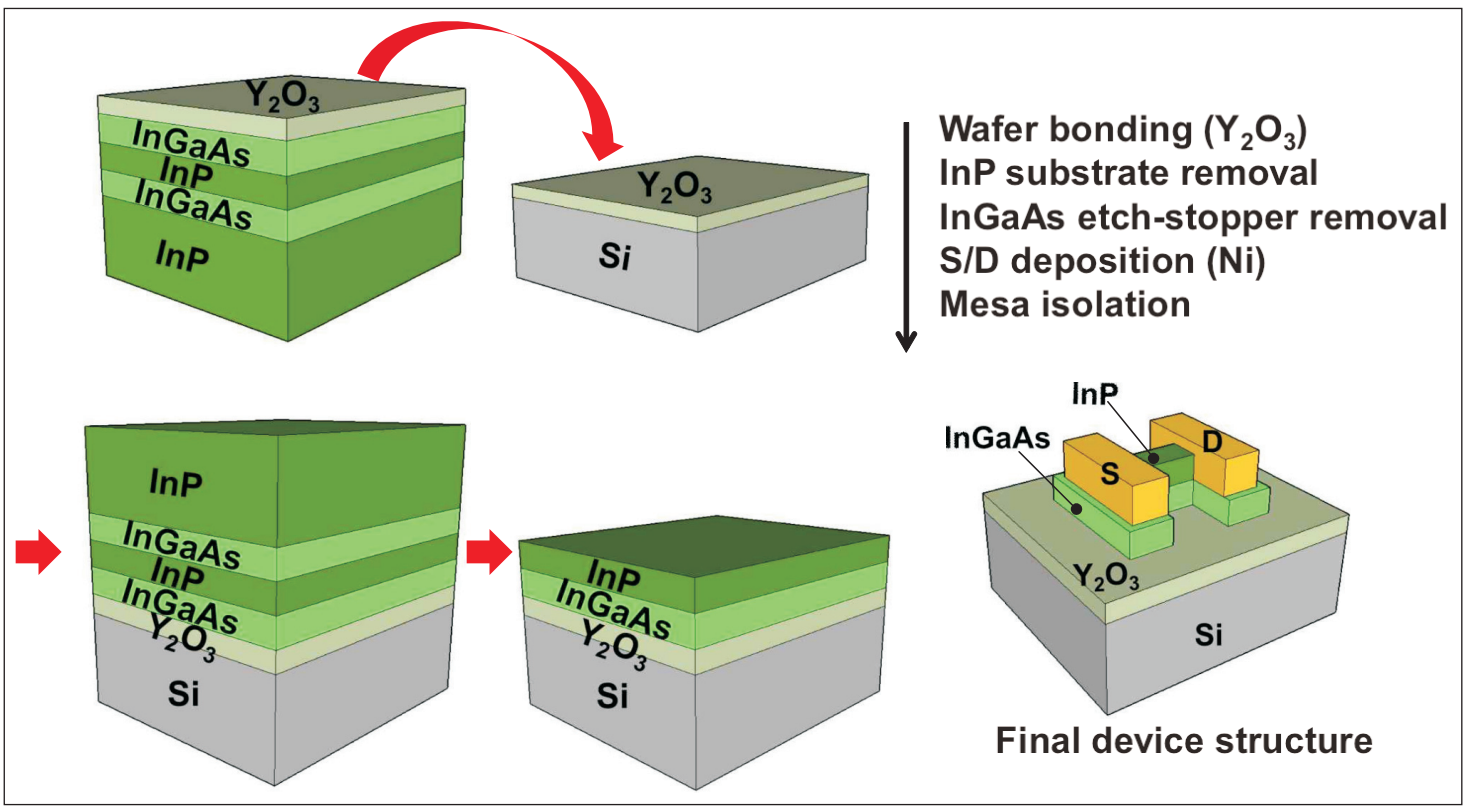

Figure 1. Fabrication process for InGaAs-OI on Si wafer by direct wafer bonding and schematic of final device.

The final device was subjected to rapid thermal annealing at 300°C. The gate length was 2μm and the body (channel) thickness was 10nm. The subthreshold swing was 90mV/decade, described by the researchers as 'very low' in view of the relatively large EOT.

The effective mobility was enhanced by a factor 2.5x over the value for silicon-based devices, even without annealing (Figure 2). Annealing at 300°C increased the effective mobility to 2000cm^2/V-s. These first results should be improvable with process optimization, according to the researchers.

The interface trap density extracted from the subthreshold behavior was 1.1x10^{12}/eV-cm^2, comparable with values from MOS capacitor measurements. These capacitor structures were produced on InGaAs/InP substrates with 10nm Y_2O_3 dielectric and top and bottom electrodes of platinum/gold and nickel/germanium/gold, respectively. Post-metal annealing at 350°C reduced interface the trap densities to as low as 4x10^{12}/eV-cm^2 near the conduction-band edge, according to capacitance–voltage measurements. Hysteresis was 15mV. ■

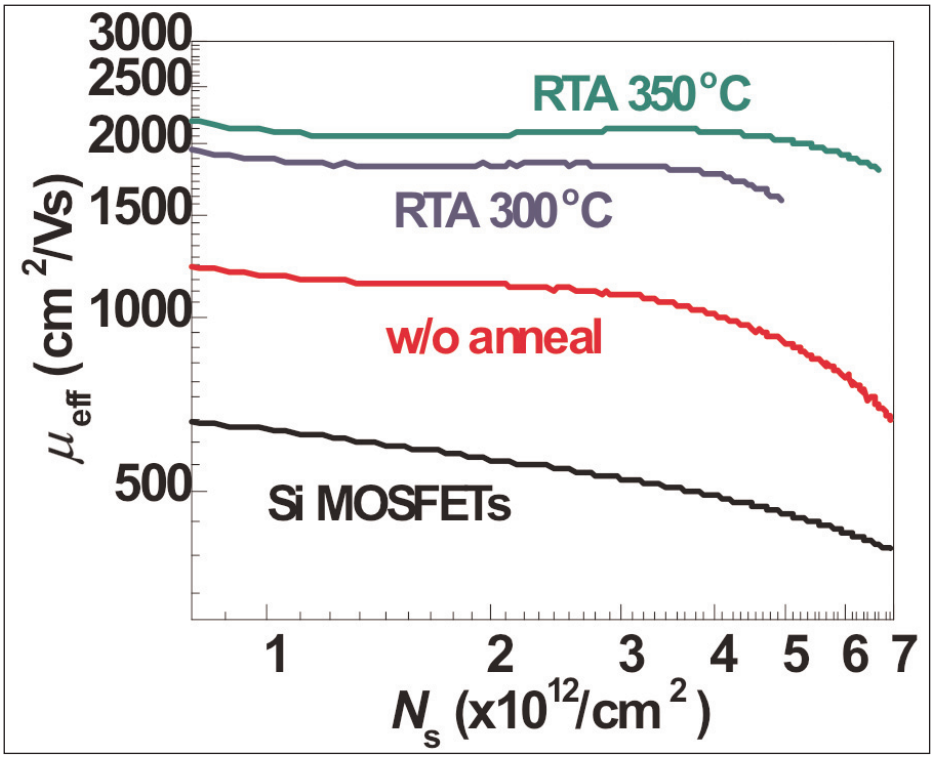

Figure 2. Effective mobility (μ_{eff}) characteristics of InGaAs-OI transistors produced with various annealing temperatures.

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