Looking to the future with III-V finFETs

Mike Cooke reports on recent separate TSMC- and IBM-led research.

Combining high-mobility III-V materials with silicon has been the subject of much research in recent years with the hope of introduction into mainstream electronics in the near future. Getting all the parts to work together at the right scale has been, is and will continue to be a challenge. Silicon is well established as the premier electronics material for low cost and seemingly ever improving speed and power performance. However, improving silicon electronics has become increasingly difficult and new processes, materials and structures have been introduced to meet expectations.

The traditional planar complementary metal-oxide-semiconductor (CMOS) transistor is presently being replaced by three-dimensional (3D) fin structures to allow better access for the gate electrode on three sides of the channel, and the next step in this progression is nanowire transistors with the gate wrapped around all four sides. Intel already uses finFETs made from silicon in some of its products (since 2011). FinFETs can be seen as intermediate between planar and gate-all-around nanowire transistors. These developments for silicon have their counterparts in III-V research.

However, some argue [e.g. Synopsis' Victor Moroz, 'Technology Inflection Points', International Symposium on Physical Design, 2016, www.ispd.cc/slides/2016/3_1.pdf] that the window of opportunity for III-V channels is closing due to large source/drain tunnel currents, which reduce on/off current ratios in the nanowire transistor gate-all-around designs that are being proposed for sub-5nm technology (circa 2021?) nodes. The tunneling currents are controlled by the effective mass. Unfortunately, high-mobility III-V materials correlate with effective masses that are too low for high-performance nanowire transistors. According to simulations, the range of effective masses needed is better covered by strained silicon.

Despite these countervailing (Cassandra?) prophecies, the European Union has set up 'Integration of III-V Nanowire Semiconductors for next Generation High Performance CMOS SOC Technologies' (INSIGHT, www.insight-h2020.eu) — a consortium under the Horizon 2020 Research and Innovation Action program.

INSIGHT involves Sweden's Lund University, the UK's University of Glasgow, Ireland's Tyndall National Institute, Germany's Fraunhofer IAF, LETI in France, and IBM Research GmbH in Switzerland. The funding is €4.3m over 36 months from 2016. The aim is to develop III-V nanowire CMOS technology for millimeter-wave applications in a system-on-chip approach, combining RF and logic for the 10nm node and beyond.

In the USA, Jesús A. del Alamo of the Massachusetts Institute of Technology leads the Xtreme Transistors Group, which recently reported record transconductance for III-V field-effect transistors (FETs) [see Mike Cooke, Semiconductor Today, p88, April/May 2016]. The MIT group aims at higher frequencies, higher speed, smaller size, extremely low power consumption, higher operating temperature, to switch electrical power, and to amplify electrical signals at higher power levels. Along with planar devices, MIT's work also includes III-V finFET and nanowire devices.

At the beginning of 2016, Taiwan Semiconductor Manufacturing Corporation (TSMC) and IBM Research GmbH reported on III-V finFETs. The finFET configuration should give better electrostatic control over channel conduction compared with planar devices like MIT's record device.

Unstrained indium arsenide

The TSMC work was led by its R&D Europe B.V. facility in Belgium. The researchers claim the first demonstration of an unstrained indium arsenide (InAs) fin field-effect transistor (finFET) with 20nm fin height (H_{fin}) [R. Oxland et al, IEEE Electron Device Letters, vol37, p261, 2016]. The team also included researchers from University of Glasgow in the UK, Texas State University in the USA, and TSMC in Taiwan.

The use of InAs rather than indium gallium arsenide (InGaAs) should increase mobility, lowering on-resistance. Since the present devices were the first of their kind, they did well to give performance comparable in some respects with scaled and optimized planar transistors.

The finFET material was grown by molecular beam epitaxy on p-InAs substrates (Figure 1). The 500nm undoped lattice-matched buffer was designed to isolate the 20nm undoped InAs channel from the conducting substrate. A quaternary indium aluminium arsenide antimonide (InAlAsSb) buffer composition gives improved top interface flatness, process and composition repeatability, and increased oxidation resistance over ternary AlAsSb, according to the

researchers. Further carrier confinement was provided by a pseudo-morphically strained 7nm InAlAs layer between the InAs channel and InAlAsSb buffer.

The fins were etched using inductively coupled plasma etch with methane, hydrogen, chlorine and oxygen chemistry. The fin height was 20nm and the width (W_{fin}) 25–35nm. The InAlAs acts as an etch stop, protecting the structure from uncontrolled oxidation, which is a particular concern for etching compound Sb-based semiconductors containing aluminium.

Before forming the gate stack, native oxide was removed

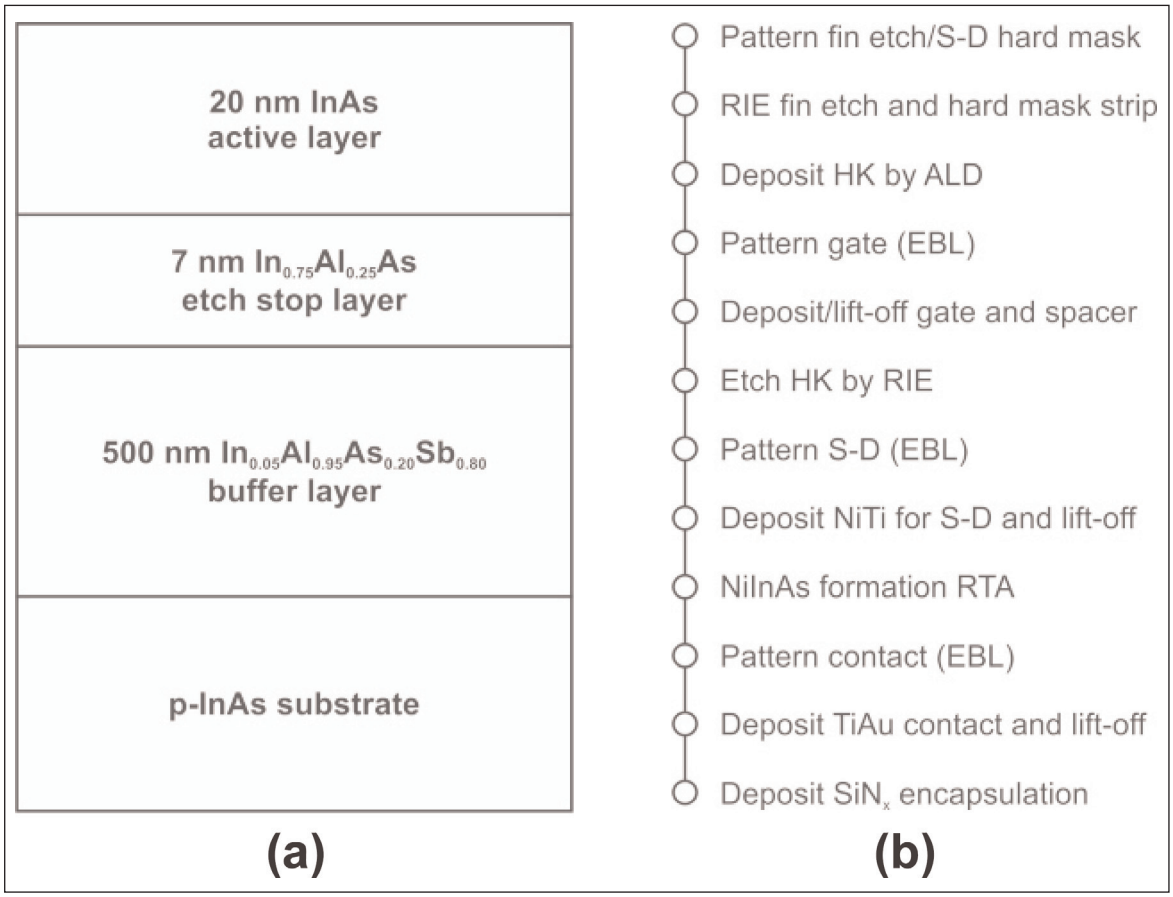

Figure 1. (a) The layer structure that was used, showing the pseudomorphic InAlAs etch stop layer and (b) the process flow for fabrication of InAs finFETs, starting with the first step after wafer growth.

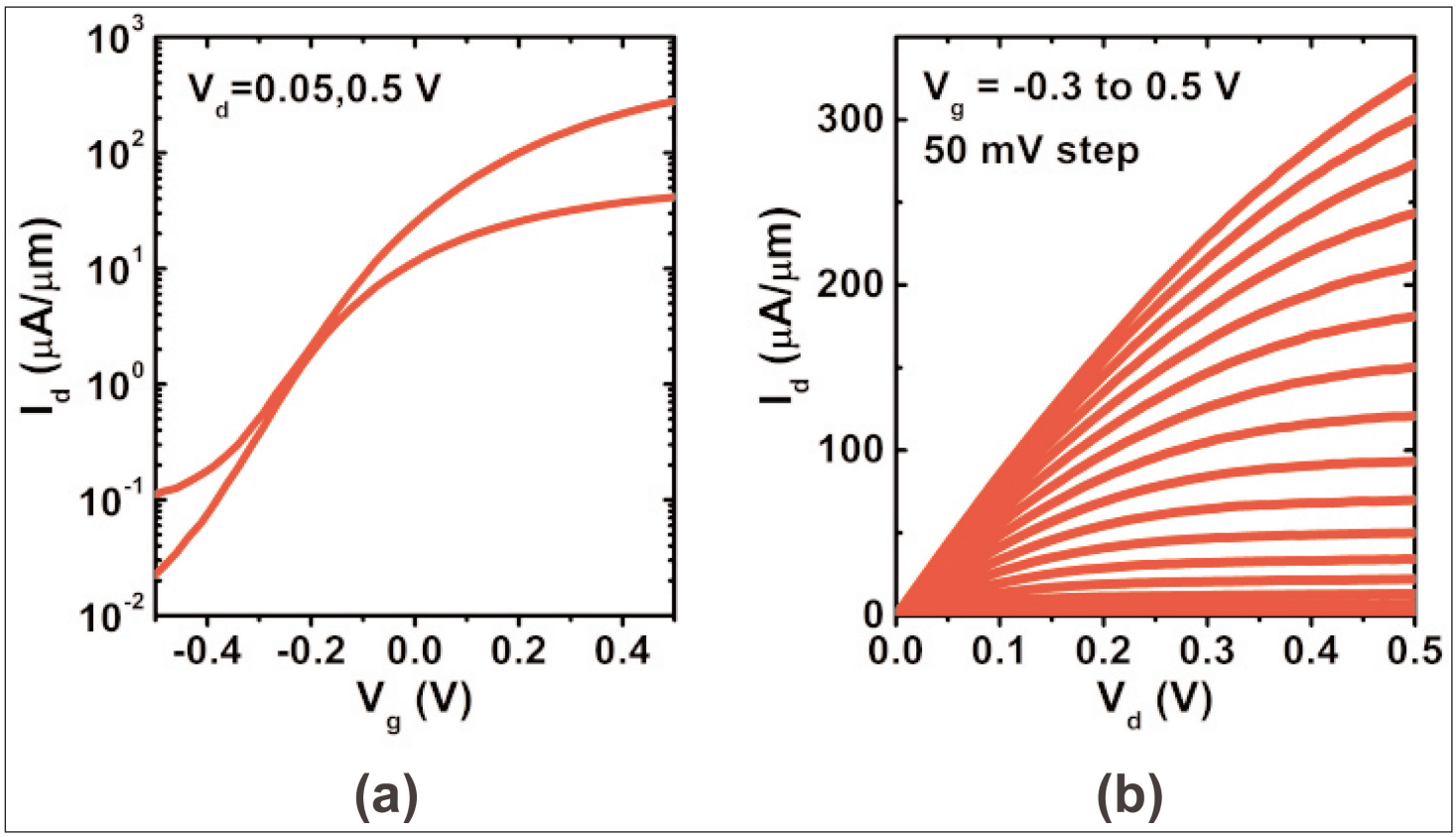

Figure 2. (a) Drain current versus gate voltage (I_d–V_g) of typical device at 0.5V and 0.05V drain bias (V_d). (b) Drain current and voltage of same device with V_g = –0.25V to 0.50V in steps of 50mV.

Table 1. Benchmark of III-V finFET devices. Quoted g_m and S values extracted at V_d = 0.5V on same device where given, otherwise not reported. Bold entry (top) is TSMC finFET. Italic entry is planar device, included for comparison. InAs channel quantum well thickness is 10nm.

InAs mole fraction	H_{fin} (nm)	W_{fin} (nm)	L_g (nm)	g_m (μS/μm)	S (mV/dec)
1.0	**20**	**25**	**1000**	**650**	**148**
		35	**1000**	**1430**	**310**
0.7	25	50	100	280	190
0.53	40	40	60	1100	95
0.53	20	30	80	1800	82
0.7	10	20	120	1620	114
0.53	16	40	200	—	150
0.53[a]	9	40	30	1640	84
1.0	—	—	*130*	*2720*	*85*

a. Mole fraction averaged over total fin height, including InAs quantum well (3nm) and $In_{0.3}Ga_{0.7}As$ cladding layers (6nm in total).

before controlled oxygen termination. The gate insulation consisted of 5nm of atomic layer deposition zirconium dioxide, giving 1.2nm equivalent oxide thickness. The gate metal was palladium. Spacers consisted of silicon nitride. The gate length (L_g) was 1μm.

The devices consisted of 10 fins. The 3μm-wide source/drain electrodes were fabricated of nickel/titanium, which was annealed to give a NiInAs metallic phase. Titanium and gold were then applied for contacts. The devices were encapsulated in 50nm of silicon nitride. The encapsulation also induced electrostatic source/drain extensions by pinning the Fermi level inside the conduction band of the InAs quantum well.

A 25nm-wide fin device had a minimum subthreshold swing (S) of 148mV/decade with 0.5V drain bias. The extrinsic transconductance (g_m) was 650μA/μm. The minimum drain current was 110nA/μm with −0.5V gate potential. Gate leakage was less than $2x10^{-8}$A/μm for the entire measurement range. The drain induced barrier lowering was 27mV/V — this compares well with the 30mV/V value of a planar InAs device of similar gate length.

A device with wider 35nm fins had 310mV/decade S and 1430μS/μm g_m with 0.5V drain. The minimum drain current of 8μA/μm occurred at −0.5V gate potential. The gate leakage was the same as for the 25nm devices. The higher off-state current was attributed to reduced gate control from the wider fin and the different interface trap densities on the sidewall and top surface.

The Q-factors g_m/S for the 25nm- and 35nm-wide finFETs were 4.4 and 4.8, respectively. The researchers compared their devices to the InGaAs finFETs of other groups (Table 1).

InGaAs on insulator

The IBM Research GmbH, Switzerland, work developed an n-channel InGaAs on insulator (-OI) finFET process and the team claims the highest on-current to date for CMOS-compatible InGaAs devices integrated on silicon (Si) [Vladimir Djara et al, IEEE Electron Device Letters, vol37, p169, 2016].

The InGaAs-OI/Si wafer was produced using metal-organic chemical vapor deposition (MOCVD) and direct wafer bonding. The 20nm $In_{0.53}Ga_{0.47}As$ layer was doped with ~$5x10^{17}/cm^3$ silicon. The buried oxide (BOX) insulator layer was 37nm thick.

Transistor fabrication (Figure 3) began with a digital wet etch of fins 15nm wide and 17nm high. A dummy gate was formed before creating 12nm silicon nitride (SiN_x) spacers with plasma-enhanced atomic layer deposition (PEALD) and dry etching.

The raised source–drain (RSD) $In_{0.53}Ga_{0.47}As$ contacts were re-grown using

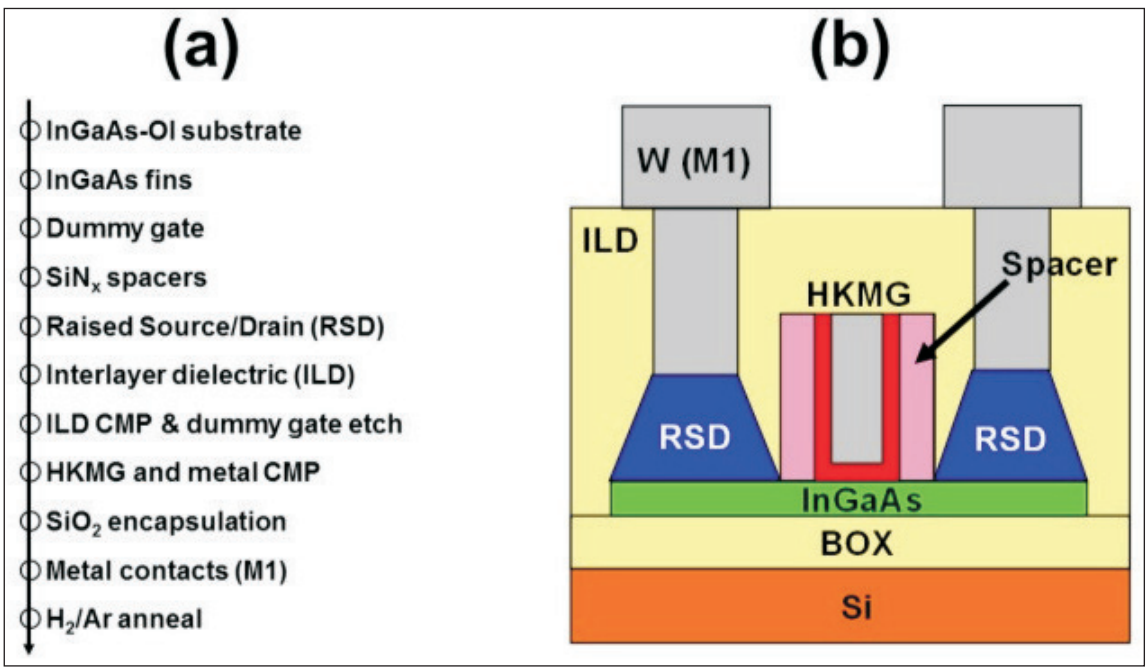

Figure 3. (a) CMOS-compatible replacement metal gate (RMG) fabrication process flow and (b) cross-sectional schematic of self-aligned InGaAs-OI FinFET architecture.

selective low-temperature MOCVD. The contacts were doped with ~$6x10^{19}/cm^3$ tin.

A 250nm interlayer dielectric was applied by plasma-enhanced chemical vapor deposition. The material was subjected to chemical mechanical polishing (CMP) that exposed the dummy gate; the dummy gate was then removed.

PEALD was used to create a high-k aluminium oxide/hafnium dioxide metal gate stack (HKMG) with a capacitance equivalent thickness of ~1.5nm. The gate metal was 150nm tungsten. This tungsten layer was planarized with CMP.

The device was encapsulated in silicon dioxide and metal contact pads created. An optimized hydrogen/argon anneal was carried out to reduce the interface trap density to ~$1.5x10^{12}/cm^2$-eV at 0.25eV below the conduction band edge, according to high-low frequency capacitance–voltage analysis.

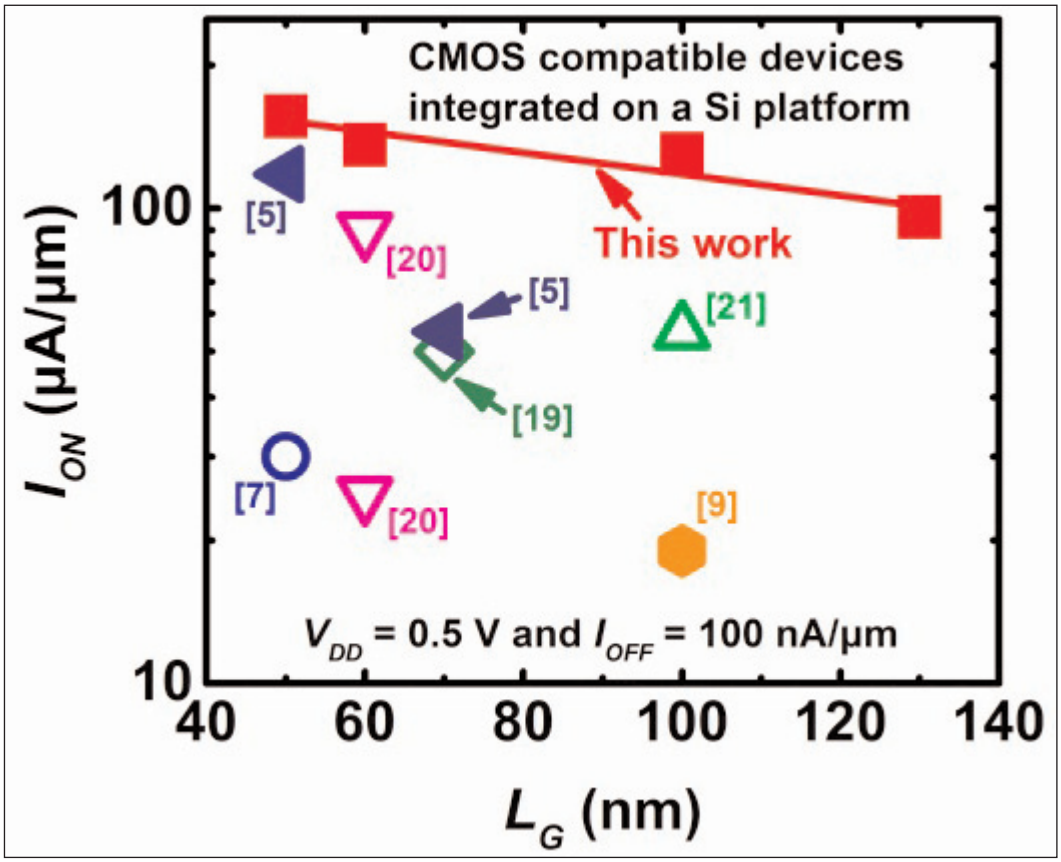

Figure 4. I_{ON} versus L_G benchmark of CMOS-compatible InGaAs FETs integrated on silicon platform. I_{ON} values are extracted at 0.5V operating voltage and an I_{OFF} of 100nA/μm.

The gate leakage current for a 50nm gate-length (L_G) transistor was below 400pA/μm with 0.5V and gate potential in the range −0.2V to +1V. The saturation transconductance peaked at ~615μS/μm. The saturation subthreshold swing had a minimum of 92mV/decade. The drain-induced barrier lowering was 57mV/V. The threshold in saturation was 0.09V.

The on-current (I_{ON}) was 156μA/μm (Figure 4). The researchers comment: "Although the I_{ON} value of 156μA/μm obtained at L_G = 50nm represents the highest value reported to date for CMOS-compatible InGaAs FETs integrated on a silicon platform, significant improvements are still needed to reach the performance of state-of-the-art III-V n-FETs integrated on bulk InP and be competitive for advanced technology nodes. We speculate that the required performance boost could be obtained through the use of source and drain extensions."

Long 1μm-gate devices had a 10^6 maximum/minimum drain current ratio and subthreshold swing of 62mV/decade. ■

The author Mike Cooke is a freelance technology journalist who has worked in the semiconductor and advanced technology sectors since 1997.