Fin structures for aluminium gallium nitride high-power electronics

Mike Cooke reports on recent research on multi-channel and vertical-current-flow devices.

Tri-gate transistors using fin nanostructures in silicon were rolled out in mass production in 2011 by Intel and other companies after many years of development. Such structures were needed to improve electrostatic control of current flow by wrapping gates around transistor conduction channels.

In recent years, researchers have applied similar fin structures to overcome problems in high-mobility III–V compound semiconductors. One application has been for high-speed transistors using materials like indium gallium arsenide or antimonide, as potential replacements for silicon-based channels.

Another direction (the topic here) has been the potential for improving the performance of high-power and high-current-flow devices, for switching applications, using gallium nitride (GaN) and aluminium gallium nitride (AlGaN) materials. These semiconductors have a wide bandgap and relatively high mobility. Such features allow for higher electric fields and hence voltages to be supported, while maintaining low on-resistance.

A problem that could be helped by wrap-around gates is converting the normally-on 'depletion-mode' performance to the more useful normally-off 'enhancement-mode'. In depletion mode, the transistor conducts when the gate is at zero potential. By contrast, enhancement-mode transistors resist current flow under a 0V gate. Normally-off behavior reduces system power consumption and also shuts off current flow when the surrounding system fails, making for safer operation in high-voltage situations.

High-mobility multi-channels on silicon

Researchers based in Switzerland and China have fabricated tri-gate metal-oxide-semiconductor high-electron-mobility transistors (HEMTs) with five III-nitride semiconductor channel levels, boosting electrostatic control and drive current [Jun Ma et al, Appl. Phys. Lett., vol113, p242102, 2018]. Fin structures were used here to enable electrical access to the deeper channels. The same team also report a Schottky barrier diode (SBD) based on similar structures [Jun Ma et al, IEEE Electron Device Letters, vol40, p275, 2019].

The team from École Polytechnique Fédérale de Lausanne (EPFL) in Switzerland and Enkris Semiconductor Inc in China sees many possible applications for lateral devices with low on-resistance and high voltage blocking enabled by tri-gate structures.

It is expected that thinner fins will allow more effective depletion under gate structures — as suggested by recent theoretical and experimental studies with Schottky gates by National Taiwan University (NTU) [Li-Cheng Chang et al, J. Appl. Phys., vol125, p094502, 2019]. Full depletion across a fin should turn a transistor off when the gate potential is zero.

The EPFL/Enkris researchers used a material structure consisting of five parallel layers of a 10nm AlGaN barrier, a 1nm AlN spacer, and a 10nm GaN channel (Figure 1). The barrier was silicon doped at a partial level of $5x10^{18}cm^3$ to enhance conductivity.

Hall measurements on the five parallel thin two-dimensional electron gas (2DEG) channels gave the sheet resistance as 230Ω/square with $1.5x10^{13}/cm^2$ carrier density and $1820cm^2/V-s$ mobility (μ). The effective resistivity (ρ_{eff}) was 2.4mΩ-cm but with small total thickness (t_{tot}). The team comments: "Small ρ_{eff} and high μ are crucial to reduce R_{ON}, and a thin t_{tot} facilitates electrostatic gate control and device fabrication (the etching of high-aspect-ratio fins and the formation of electrodes around them can be challenging)."

The tri-gate structure was achieved with patterned inductively coupled etching to a depth of 200nm. The ohmic source/drain contacts consisted of annealed titanium/aluminium/titanium/nickel/gold. The gate stack was 25nm atomic layer deposition (ALD) silicon dioxide insulator and nickel/gold electrode.

One device had a gate length of 51μm: 50μm fin length and two 0.5μm extensions towards source and drain. Control of the channel current was affected by the fin width. In particular, with wide fins, control of the deeper channels was sluggish. This was shown by the transconductance exhibiting five peaks, one for each channel, when the width was greater than 200nm. (Consistent with the NTU study on Schottky gates that found an "early pinch-off effect" for

narrower fins.) The peaks merged at 40nm width. The 40nm device demonstrated a small negative threshold of –0.08V, improved subthreshold swing of 101mV/decade, and 29.5mS/mm peak transconductance.

Of course, reducing fin widths tends to reduce drain current in the on-state. The multiple channels compensate for this somewhat. The maximum current decreased steadily as the fin width was reduced in single-channel devices, while for 5-channels the impact was only apparent for widths less than 200nm. With 100nm-wide fins, the single-channel current was reduced by 41% relative to a planar gate; the 5-channel reduction was only 12%.

The researchers explain that "the multi-channel structure mitigates greatly the electron–electron and sidewall scatterings in tri-gate (MOS)HEMTs." The electrons in single-channel devices are tightly packed, increasing the rate of electron–electron collisions and hence resistance. Further resistance comes from more electrons hitting the fin sidewalls. Multi-channel structures reduce electron crowding in the separate channels.

A high-voltage MOSHEMT was produced with 10μm gate–drain spacing, and 700nm-long, 100nm-wide fins. The spacing between the fins was 100nm, giving a fill factor of 50%. The gate metal extended 0.5μm towards the source and 1.3μm in the drain direction, giving a total length of 2.5μm.

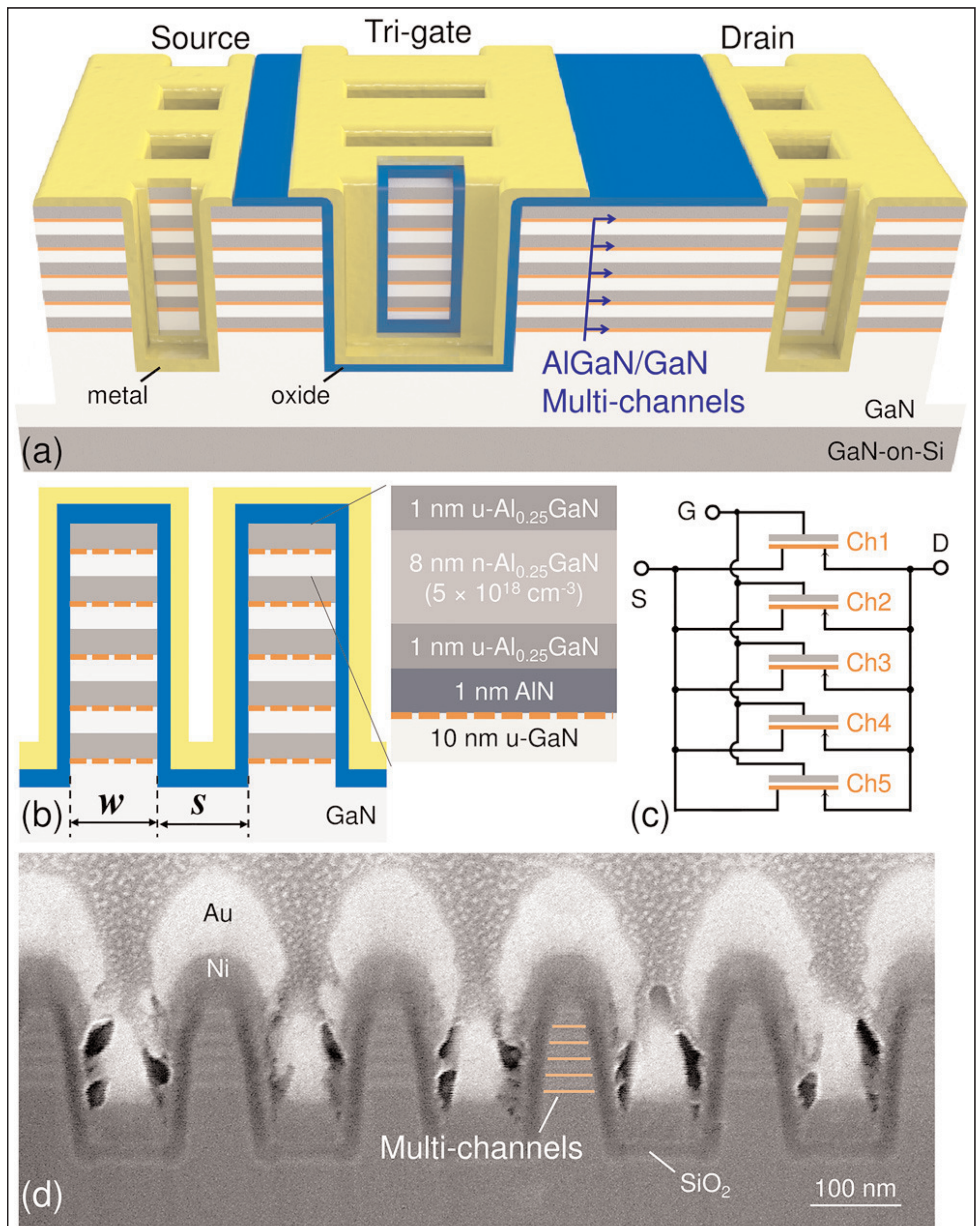


Figure 1. (a) Schematic of multi-channel tri-gate AlGaN/GaN MOSHEMT. (b) Cross-sectional schematic of tri-gate region. Inset shows multi-channel heterostructure. (c) Equivalent circuit. (d) Cross-sectional scanning electron microscope image of tri-gate region, tilted by 52º.

Two single-channel reference devices were fabricated with similar dimensions: one with planar- and the other with tri-gate structures. The barrier layer in these reference devices was a typical 20nm of $Al_{0.25}Ga_{0.75}N$ on GaN channel.

The multi-channel tri-gate devices showed reduced on-resistance (Figure 2). Compared with the single-channel tri-gate reference, the on-resistance was almost half, and the maximum drain current increased more than three-fold. Normalized by the device width, the on-resistance was 6.0Ω-mm for the multi-channel MOSHEMT, compared with 11.2Ω-mm for the single-channel device. The multi- and single-channel maximum drain currents were 797mA/mm and 252mA/mm, respectively.

The team comments: "These results are remarkable since they indicate that the multi-channel tri-gate technology can lower the conduction losses of the transistor for a given device footprint or, equivalently, deliver a given current rating in a smaller device footprint, both of which are highly beneficial for efficient power transistors."

Compared with the planar reference, the multi-channel MOSHEMT had 38% reduced on-resistance and 41% increased maximum drain current. This was despite the 50% fill factor of the fin structure, compared with the 100% of the planar setup.

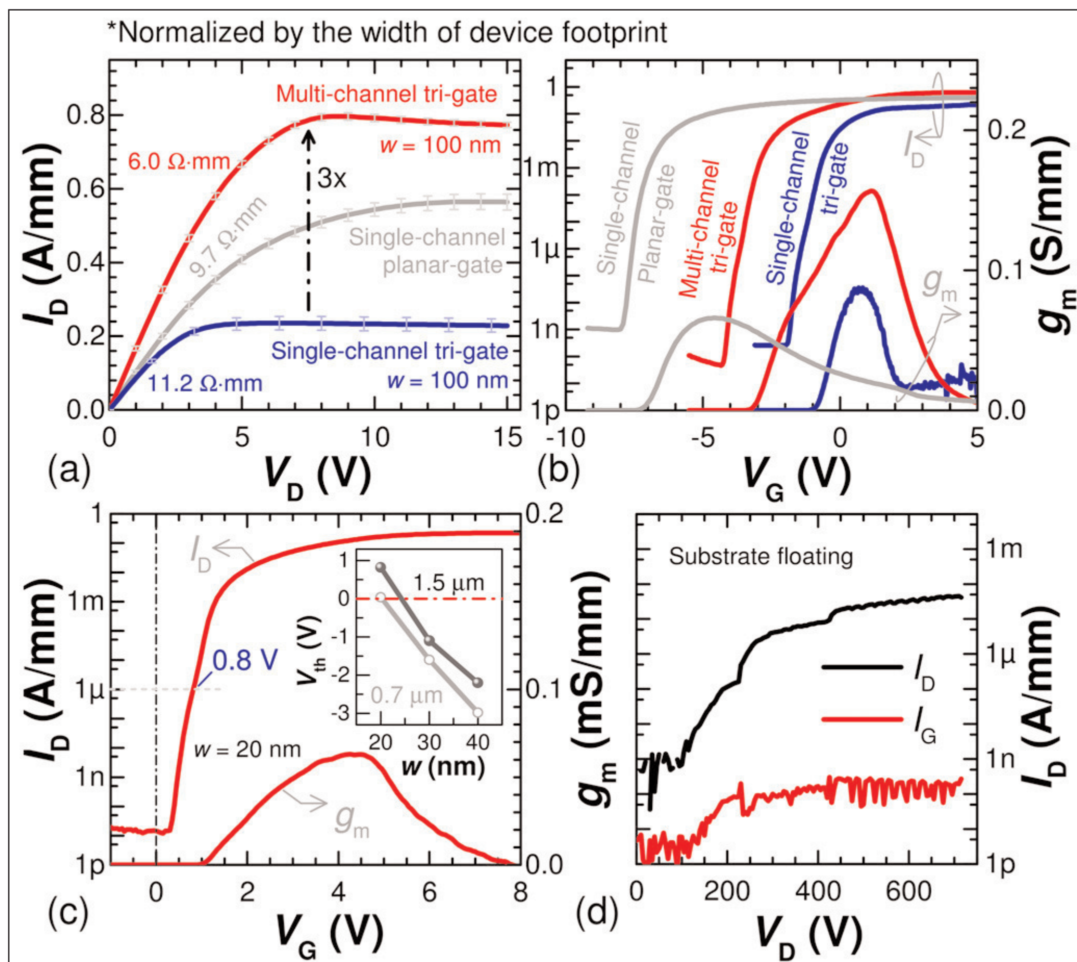


Figure 2. (a) Output characteristics at 5V gate potential (V_G) and (b) transfer characteristics at 5V drain bias (V_D), normalized by width of device footprint. (c) Transfer characteristics of multi-channel tri-gate transistors with 20nm fin width and 10% fill factor at 5V V_D. Inset threshold voltage (V_{TH}, for 1μA/mm current) versus fin width (w) for two fin lengths (l).(d) Typical OFF-state breakdown characteristics of multi-channel tri-gate transistors measured with floating substrate.

The threshold voltage was made more positive by moving from the planar reference to the multi-channel fin MOSHEMT, going from −7.6V to −3.6V, respectively. The peak transconductance also increased 2.4-fold in the multi-channel device — 156.6mS/mm, compared with 66.1mS/mm. The on/off current ratio of the multi-channel MOSHEMT was ~10^{10}.

Using a 20nm fin width (700nm length), the researchers achieved a positive threshold voltage of 0.82V a 1μA/mm. The off-current at 0V gate potential was 12pA/mm. Positive thresholds are desired for normally-off, enhancement-mode operation. The researchers attribute the positive threshold to the sidewall depletion effect. For longer 1.5μm fins, the sidewall depletion fin width was slightly increased to 24nm, likely due to increased strain relaxation relative to shorter fins.

Hard off-state breakdown came at 715V, while the gate leakage was still of order 0.2nA/mm at 700V drain bias.

Reducing Schottky on-resistance

The EPFL/Enkris lateral Schottky barrier diodes (SBDs) also used tri-gate multi-channel AlGaN heterostructures on silicon. The team comments: "This unique design significantly enhanced the device performance, leading to state-of-the-art lateral GaN-on-Si power SBDs, and unveiled a novel platform to drastically improve the efficiency, increase the current rating, and reduce the size of GaN-based power devices."

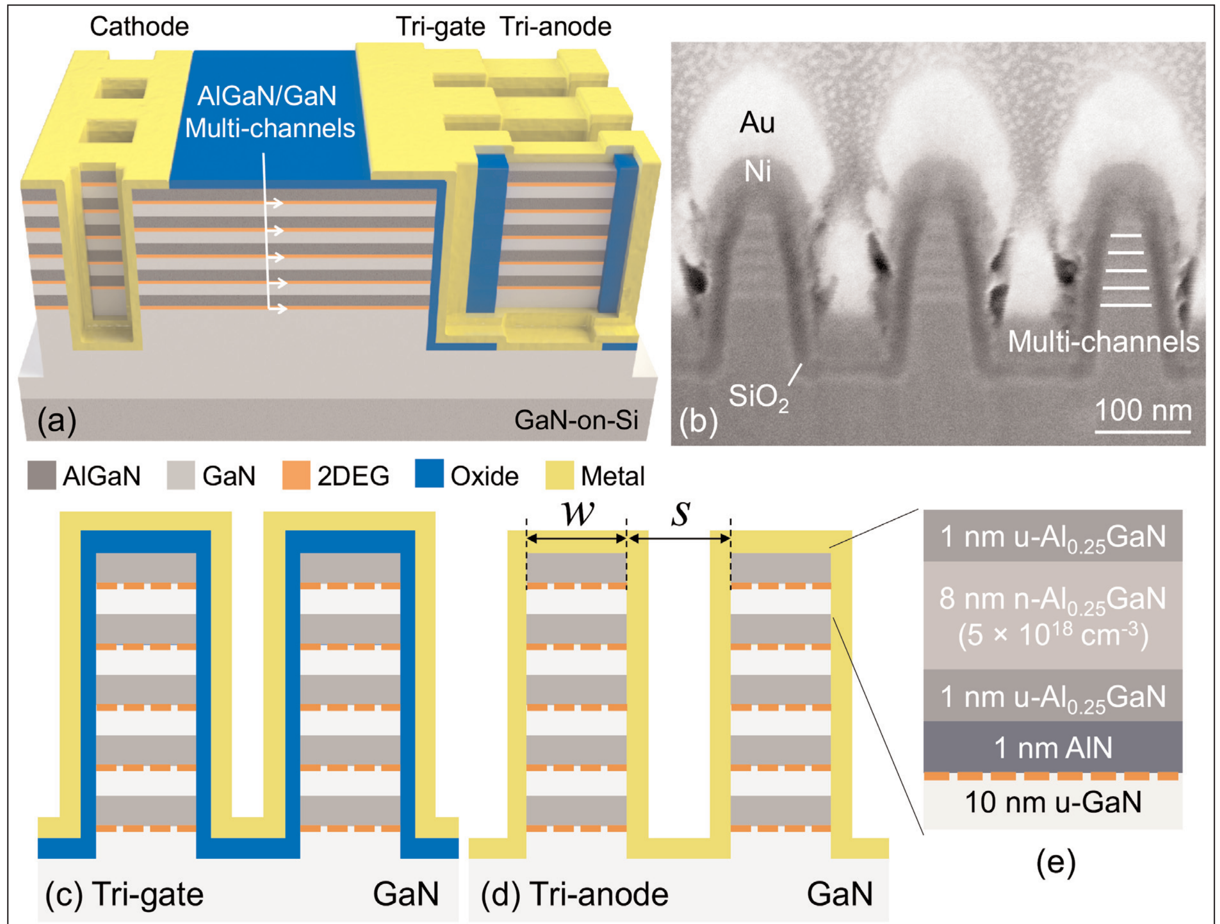
The multi-channel material consisted again of 5 layers of 10nm/1nm/10nm AlGaN/AlN/GaN grown on silicon with a 4.3μm buffer layer (Figure 3). The electrical performance was identical in terms of sheet resistance, carrier density and mobility — presumably the same epitaxial material was used in both experiments.

Fin structures were etched to enable access to the multi-channels. The nickel/gold (Ni/Au) Schottky anode comprised 200nm-high and 50nm-wide fins with 1.2μm oxide-insulated tri-gate and 4μm tri-anode regions. The tri-gate region served as a field plate to reduce peak fields and enhance breakdown performance. The gate structure also extended into the planar region, operating as a second field plate. The gate insulator was 25nm atomic layer deposition (ALD) silicon dioxide. The cathode-anode spacing was 15μm. The fins in the cathode region were 500nm wide with 500nm spacing.

A single-channel reference device was produced based on material with $1 \times 10^{13}/cm^2$ carrier density and $2000cm^2/V\text{-}s$ mobility. The multi-channel device had ~50% reduced on-resistance (R_{ON}), compared with the single-channel performance. Also, the forward voltage for 0.1mA/mm current was reduced from 2.21V to 1.57V for the single- and multi-channel SBDs, respectively. The turn-on voltage of both devices was around 0.67V.

The reverse current of the multi-channel device (0.89nA/mm at −100V) was around six times smaller than for the single-channel structure. At 150ºC, the

Figure 3. (a) Schematic of multi-channel tri-gate SBD. (b) Cross-sectional scanning electron microscope image of tri-gate region, tilted by 52º. Cross-sectional schematics of (c) tri-gate and (d) tri-anode regions. (e) Schematic of heterostructure composing each channel.



reverse current at −100V was 86nA/mm for the multi-channel SBD. With grounded substrate, the multi-channel SBD had a 1μA/mm break-

Figure 4. Specific on-resistance ($R_{ON,SP}$) versus V_{BR} benchmark of multi-channel tri-gate SBDs against state-of-the-art lateral GaN SBDs. Some values were recalculated for fair comparison.

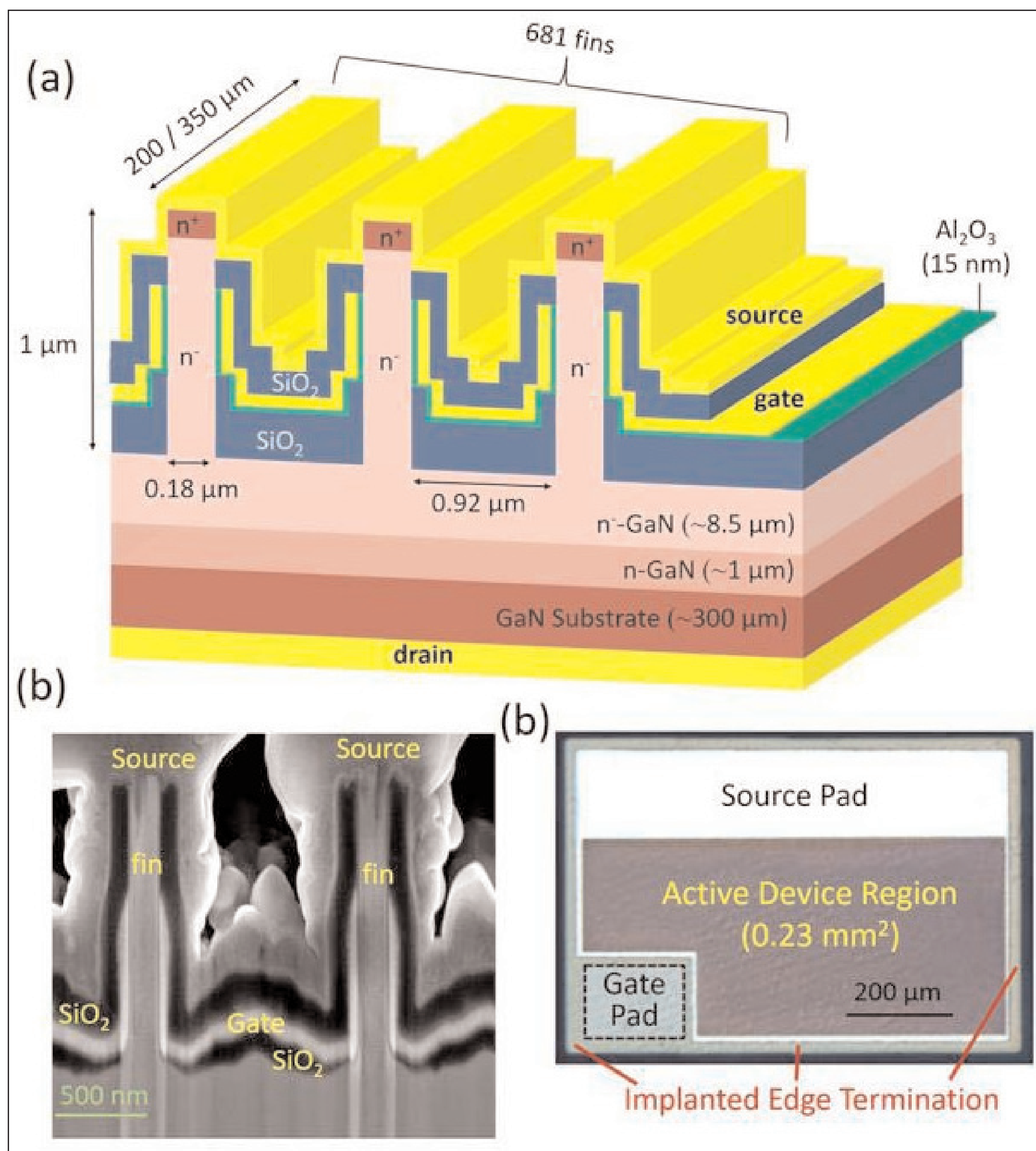


Figure 5. (a) Three-dimensional schematics of GaN vertical power FinFETs with multiple fin channels. (b) Cross-sectional scanning electron microscope (SEM) image of fin area, taken in focused ion beam system. (c) Optical microscope image.

down voltage (V_{BR}) of 900V. At –650V reverse bias, the leakage current (I_R) was ~3nA/mm. "Such high voltage-blocking performance indicate the potential of these devices for 650V applications, providing a small I_R at the rated voltage and a safety margin of ~50% from the rated voltage to the hard breakdown," the researchers comment.

The V_{BR}^2/R_{ON} power figure of merit was 1.25GW/cm^2. The team says that this is comparable to state-of-the-art GaN-on-GaN vertical SBDs and GaN-on-silicon transistors (Figure 4).

The recovery times at 1MHz were 13.8ns and 8.2ns in the forward and reverse directions, respectively. These values were stable between 10kHz and 10MHz. However, a phase shift between voltage and current became apparent above 5MHz.

Boosting switching frequency in vertical transistors

Fins have also been used in vertical device structures. Researchers based in USA and Singapore claim a record switching figure of merit for large-area 1.2kV GaN vertical power fin field-effect transistors (FETs) [Yuhao Zhang et al, IEEE Electron Device Letters, vol40, p75, 2019]. The team from Massachusetts Institute of Technology in the USA, the Singapore–MIT Alliance for Research and Technology in Singapore, and IQE RF LLC and Columbia University in the USA writes that this was "the first experimental study on capacitances, charges and power-switching figure of merits (FOM) for a large-area vertical GaN power transistor."

Vertical GaN structures should enable higher breakdown voltages in smaller dimensions with easier thermal management. The team reported on their design over a year ago at the International Electron Devices Meeting 2017 [Mike Cooke, Semiconductor Today, vol12, issue 10, p98, Dec 2017/Jan 2018]. The device uses only n-type material, making for easier epitaxial growth and reducing charge-storage problems. Normally-off performance is enabled by the fin structure in combination with the gate-metal work function producing full depletion of the channel at zero gate potential. Normally-off operation reduces power consumption and further allows for easy shut-off after failure.

The latest development of this device structure incorporated argon-implant edge termination under the gate pad edges "for the first time in vertical GaN FinFETs".

The researchers used metal-organic chemical vapor deposition (MOCVD) on 2-inch heavily n-doped GaN substrates. The lightly doped n^--GaN drift layer was ~9.5µm. The heavily doped n^+-GaN cap was 300nm.

The epitaxial material was fabricated into devices (Figure 5) with 489 350µm-long fins and 183 200µm-

long fins (the gate pad region). The active device area was $0.23mm^2$. Adding pads and so on, increased the area to $0.45mm^2$.

The process sequence was fin etch and corner rounding, argon-implantation edge termination, spacer oxide deposition, and formation of gate, source and drain contacts.

The resulting device had a threshold voltage of +1.3V at 2mA drain current. The researchers report that there was almost no hysteresis in the threshold with up and down sweeps. The drain current was able to reach 5A and the on-resistance was 0.9Ω, giving an active-area specific value of $2.1m\Omega\text{-}cm^2$.

The reverse turn-on voltage was 0.8V, lower than usual for silicon carbide or GaN devices (2–3V). The team attributes this to the absence of pn junctions in the epitaxial material. The low turn-on implies lower power losses, and in some cases this could "eliminate the need for paralleling a freewheeling diode in many switching applications". Destructive breakdown occurred above 1.2kV. Just before breakdown the leakage current was at the micro-Amp level.

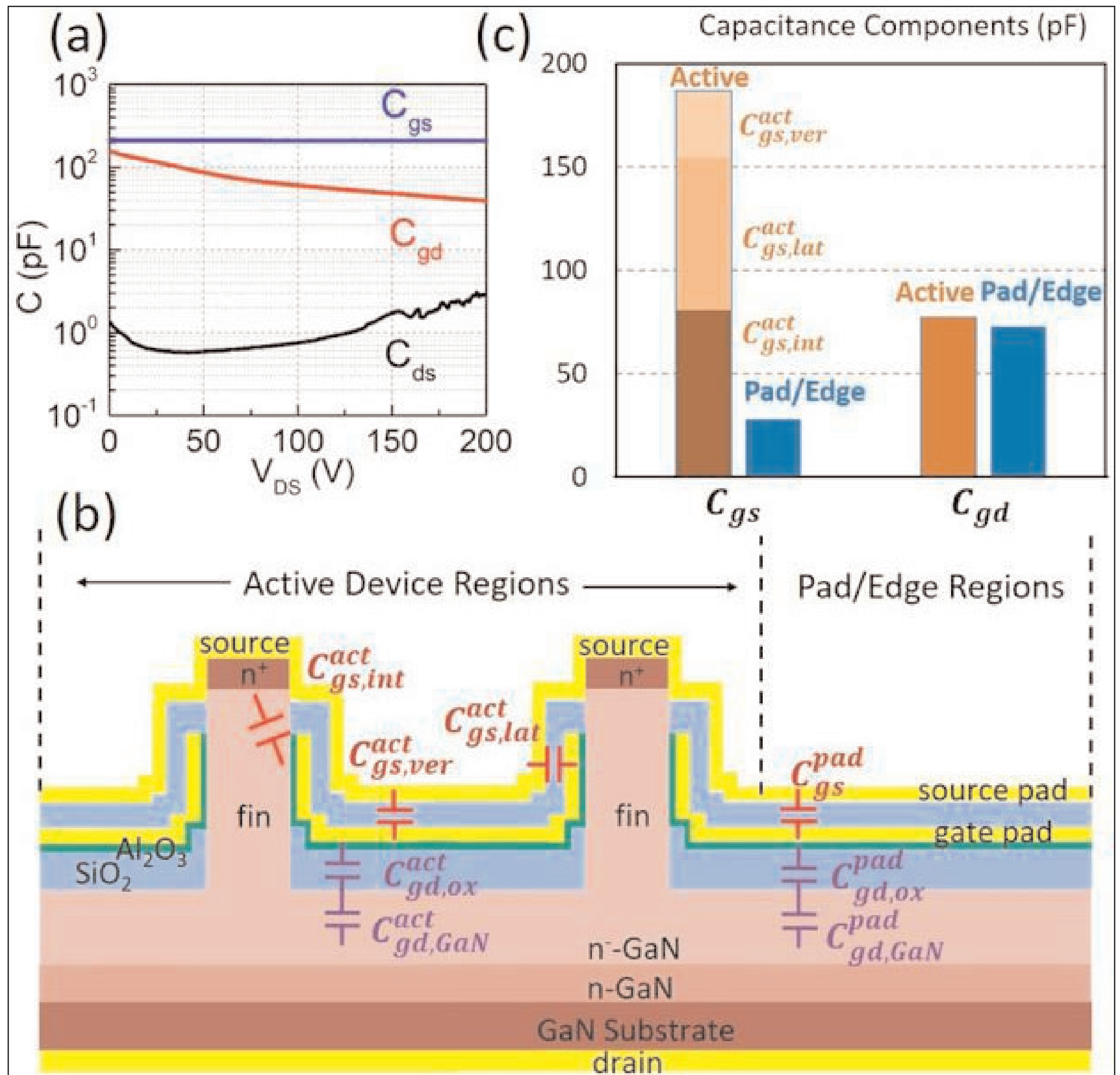


Figure 6. (a) Device junction capacitances C_{ds}, C_{gs} and C_{gd} measured by using Agilent B1505A power device analyzer and custom-built RC circuit. (b) Schematics of different C_{gs} and C_{gd} components in active and pad/edge regions. (c) Calculated components break-out for measured C_{gs} and C_{gd}.

The researchers estimate that switching speeds for their device could reach ~3.5MHz on the basis of the on-resistance and charge-storage performance. The greater the charge stored in parasitic capacitors (Figure 6), the more difficult it is to switch states. A figure of merit (FOM) based on the product of the on-resistance and gate and gate–drain charge was calculated at 3.3nΩ-C. The researchers believe this could be reduced to around 2nΩ-C if the contact pads were optimized. A low value should enable higher switching speeds.

The team also reports the FOM for other devices: 7.68nΩ-C for Cree's CPM2-1200-0160B silicon carbide MOSFET, 5.4nΩ-C for United SiC's UJN1208Z JFET, 54.5nΩ-C for ON Semi's NGTB15N120FLWG insulated-gate bipolar transistor, and 48nΩ-C for Infineon's IPD90R1K2C3 silicon CoolMOS device. These devices also have significant reverse-recovery charge storage (Q_{rr}) problems due to the presence of p-type regions. Including this charge increases the FOMs to 24.48nΩ-C, 14.85nΩ-C, 429.5nΩ-C, and 4488nΩ-C, respectively. By contrast, since there is no p-type material in the team's FinFET, the reverse-recovery charge is effectively zero.

The researchers comment: "As shown, our device exhibited the best power switching FOMs among all 0.9–1.2kV power transistors. This is attributable to the combination of the superior physical properties of GaN and the merits of our vertical FinFET (small capacitances, low V_G [gate potential] and no Q_{rr})." ■

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