Extreme-k and Ga_2O_3 power moves

Barium titanate layer massages peak electric field pain in lateral transistors.

Ohio State University in the USA has claimed the highest reported power figure of merit for gallium oxide (β-Ga_2O_3) lateral transistors of 376MW/cm^2 [Nidhin Kurian Kalarickal et al, IEEE Transactions on Electron Devices, vol68, Issue 1 (January 2021), p29]. The researchers used an insulator consisting of barium titanate ($BaTiO_3$), a perovskite oxide that combines an extreme dielectric constant with high breakdown field strength (>8MV/cm).

The dielectric enabled a reduction in peak fields for a given bias, according to simulations. Radio frequency (RF) and power electronics could benefit from higher average electric fields enabling better efficiency, power density, and faster speed.

The team comments: "The integration of extreme permittivity dielectrics based on perovskite oxides into conventional and wide-bandgap semiconductors such as Si, GaAs, GaN and SiC could enable unprece-

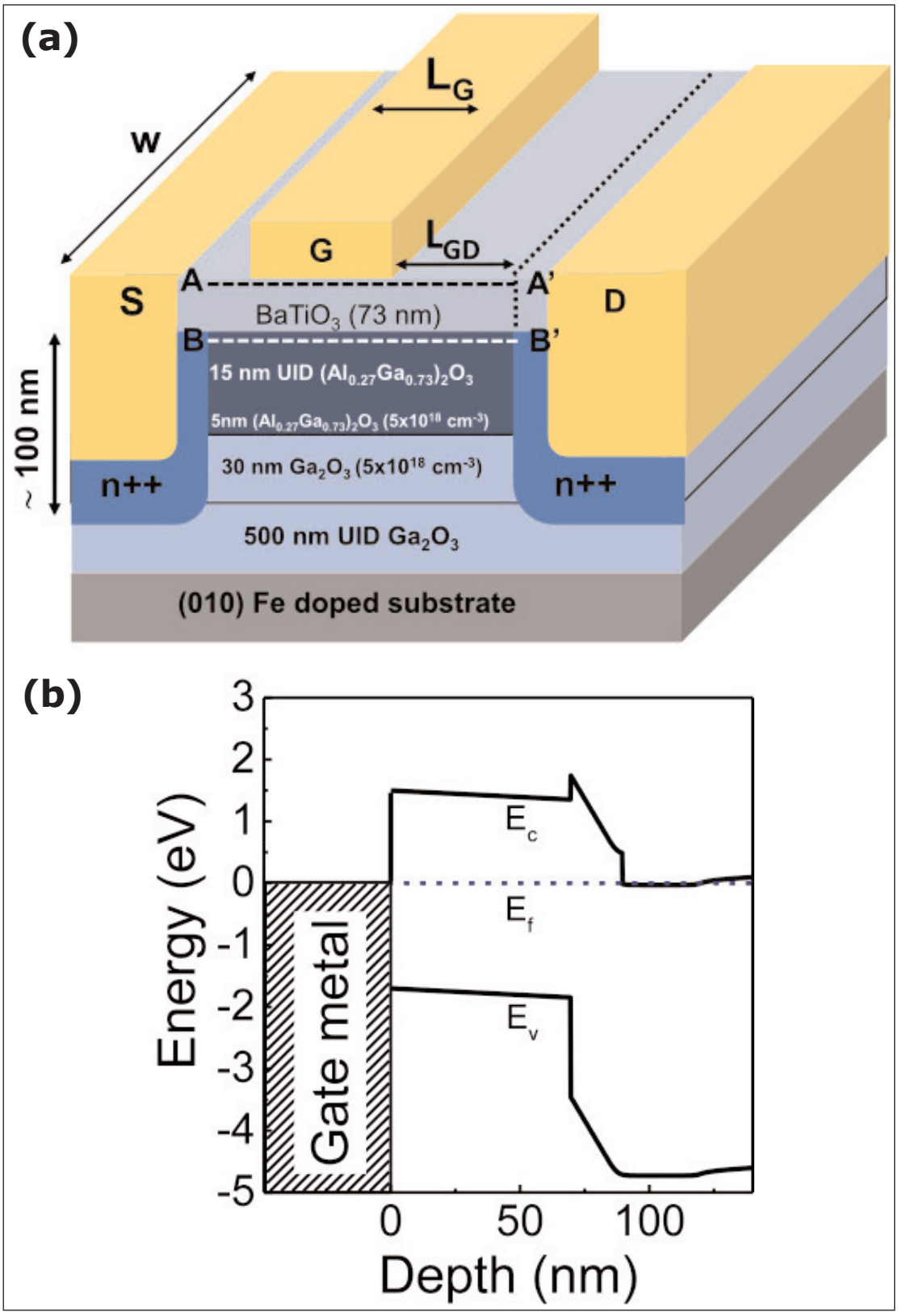

Figure 1. (a) Epitaxial/device diagram of $BaTiO_3$/β-Ga_2O_3 MISFET. (b) Simulated band diagram along vertical cutline through gate.

dented performance improvements in RF and power electronics devices."

The use of the $BaTiO_3$ dielectric also enabled a higher channel charge density of 1.6x1013/cm^2, reducing on-resistance. The β-Ga_2O_3 has a theoretical breakdown field strength of 8MV/cm, which is much greater than the 3MV/cm for gallium nitride (GaN). One drawback of β-Ga_2O_3 is a lower mobility. This can be compensated for somewhat with the higher channel charge.

The researchers fabricated lateral metal–insulator–semiconductor field-effect transistors (MISFETs) on β-Ga_2O_3 with extreme-k $BaTiO_3$ as the insulator (Figure 1). The channel region was formed using 880°C metal-organic chemical vapor deposition (MOCVD) of β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ layers on iron-doped β-Ga_2O_3 substrate. The 5x10^{18}/cm^3 intentionally doped aluminium/gallium oxide layers were achieved with silicon from silane (SiH_4).

Source and drain regions were defined using optical lithography followed by silicon ion implantation and activation by 900°C annealing for 30 minutes. The source and drain were then etched down to the β-Ga_2O_3 and annealed metal contacts formed from titanium/gold/nickel.

The $BaTiO_3$ was applied using 670°C RF sputtering from a sintered $BaTiO_3$ source. The $BaTiO_3$ was 73nm thick, a little short of the 75nm target. The sputtering had a negative effect on the channel resistance, which the researchers hope could be ameliorated in the future with an Al_2O_3 interlayer to avoid sputter damage. The source/drain ohmic contacts also suffered from sputter degradation, which could be improved by applying the metals after the $BaTiO_3$ and/or by optimizing the metal stack.

The device was completed with mesa isolation etching and deposition of a nickel/gold/nickel Schottky gate. The gate–drain spacings (L_{gd}) ranged from 0.5μm to 6μm. The gate length was 0.7μm.

Capacitance–voltage measurements suggested a dielectric constant of 235 for the $BaTiO_3$, but the team comments: "This is only a lower bound estimate on the dielectric constant since there is a small depletion of charge in the channel after the deposition of $BaTiO_3$. Nevertheless, the lower bound estimate of 235 is high enough to ensure electric field management."

The lowest on-resistance was 13.6Ω-mm, normalized to the gate width with 0.5μm L_{gd} and 1.5μm L_{sd}. The drain current reached 359mA/mm — "the highest reported in any epitaxially grown β-Ga_2O_3 lateral transistor device under dc conditions, and higher currents have only been obtained in β-Ga_2O_3 nanomembrane transistors transferred onto high-thermal-conductivity substrates like diamond and Si," according to the team.

The three-terminal breakdown voltage (V_{br}) increases with L_{gd}, with the highest value being 918V for 6μm spacing. For 0.5μm Lgd breakdown occurred at 201V. The average field at breakdown reduced from 4MV/cm at 0.5μm Lgd to 1.5MV/cm at 6μm.

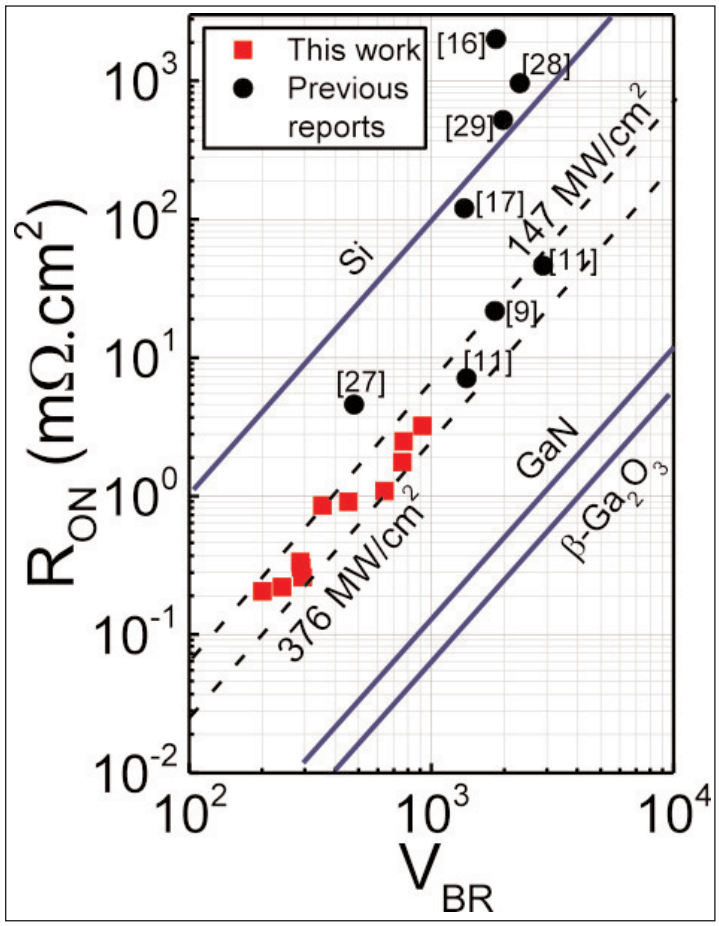

Figure 2. Benchmark plot against previous β-Ga_2O_3 lateral transistor reports.

Reverse-bias current measurements suggested that gate leakage limited the breakdown performance. Simulations showed a spike in electric field at the gate corner, which in the device would increase gate current leakage and result in dielectric breakdown.

The power figure of merit V_{br}^2/R_{spON} balances the trade-off of breakdown and specific on resistance, normalized to the source–drain area (L_{sd} x width). The devices all achieved a value for this figure of merit greater than 147MW/cm^2, reaching 376MW/cm^2 for 4.7μm L_{sd} and 3μm L_{gd}, which had 640V V_{br} and 1.08mΩ-cm^2 R_{spON}. The team claims the 376MW/cm^2 figure as "the highest reported value for any β-Ga_2O_3 transistor to the best of our knowledge" (Figure 2).

The researchers comment: "The extreme-k field management strategy using $BaTiO_3$as the gate dielectric has thus resulted in superior performance even in the absence of additional field termination structures like field plates."

The team hopes that future devices could include such termination to further improve performance. ■

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