

Split gate improves octagonal-cell silicon carbide MOSFET performance

Reduced capacitance and charge storage figures of merit show the first 1.2kV silicon carbide devices with better performance than 600V silicon-based power transistors.

Kijeong Han and B. J. Baliga of North Carolina State University (NC State) in the USA have combined split-gate structures with their 1.2kV-rated octagonal-cell (OCTFET) layout for 4H-polytype silicon carbide metal-oxide-semiconductor field-effect transistors (MOSFETs) "for the first time" [IEEE Electron Device Letters, vol40, issue 7 (July 2019), p1163].

Han and Baliga reported late last year on the advantages of OCTFET over linear-cell layouts in terms of improved high-frequency figures of merit (HF FOMs) [www.semiconductor-today.com/news_items/2019/feb/ncsu_010219.shtml]. The junction field-effect transistors (JFETs) were designed to operate in accumulation-mode rather than inversion-mode due to higher channel mobility.

The split-gate addition in the latest work removes some gate metal from over the JFET region, decreasing

capacitance and charge storage due to reduced gate-to-drain overhang, X (Figure 1). Han and Baliga explain: "The minimization of reverse transfer capacitance (C_{rss} or C_{gd}) and gate-to-drain charge (Q_{gd}) of the devices is beneficial for improving high-frequency performance because they are dominant factors that determine switching energy loss."

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The devices (were fabricated at a 6-inch SiC power MOSFET foundry run by X-FAB in Texas. The 6-inch 4H-SiC substrate included a 10 μ m n-SiC epitaxial layer. While

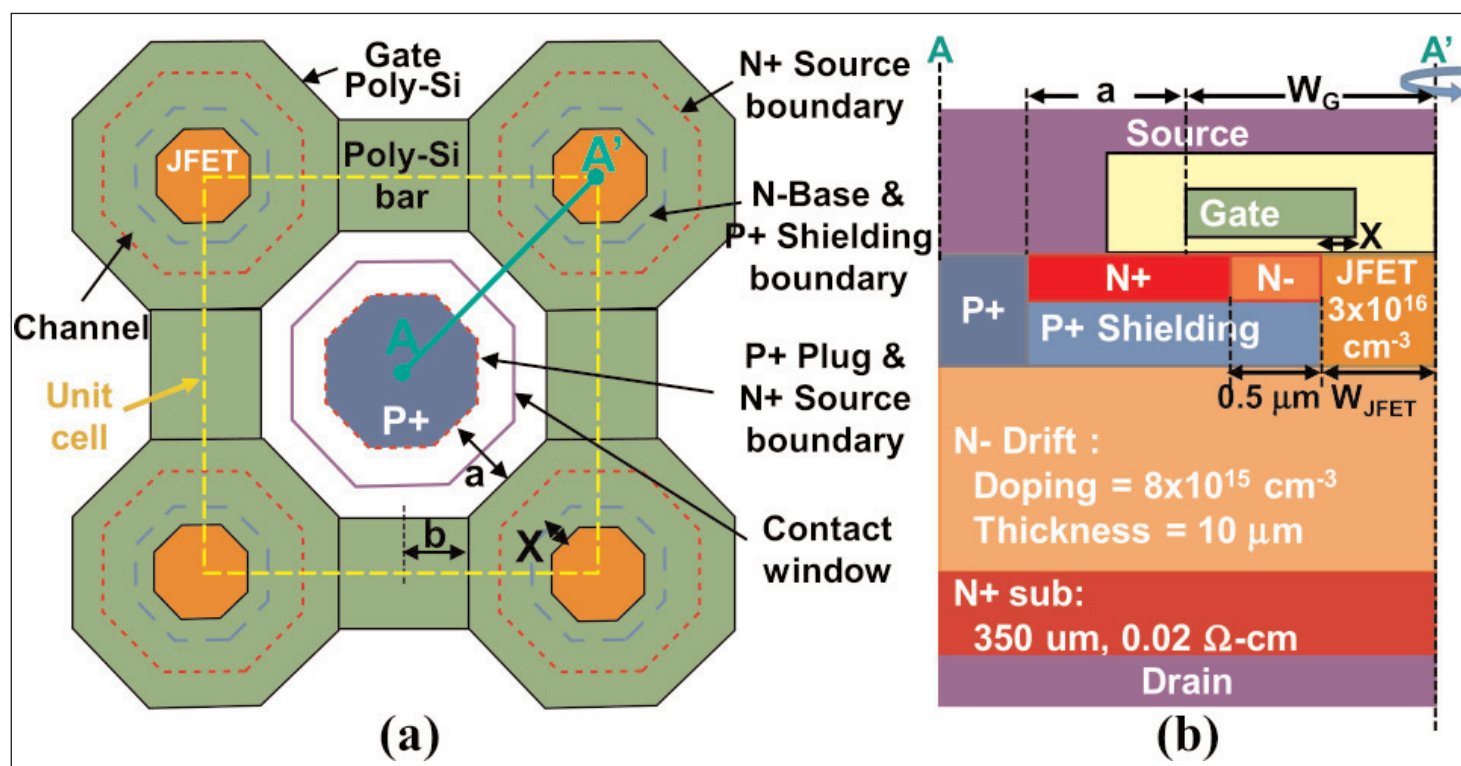


Figure 1. (a) Split-gate OCTFET (SG-OCTFET) cell layout topology. (b) Split-gate MOSFET cell cross-section at A-A' in SG-OCTFET.

the substrate was heavily n-doped, the epitaxial layer was lightly doped to give a drift layer. The gate electrode and MOSFET connecting links consisted of polysilicon (Poly-Si).

Simulations were used to optimize the dimensions of the split-gate OCTFET cell:

WJFET=1.5 μ m,
a=1.1 μ m, X=0.3 μ m. The trade-offs for X included low on-resistance (large X favored) and low capacitance (low X).

To keep the peak electric field down, the X value should also avoid the region 0.7–0.9 μ m,

where the expected peak field was of order 4.4MV/cm. For a peak field of less than 4MV/cm, and low HF-FOM values, the X value should be less than 0.3 μ m.

The split-gate OCTFET was found to have reduced gate–drain capacitance-charge storage, as represented in the HF-FOMs combining specific on-resistance with gate–drain capacitance and charge storage ($R_{on}C_{gd}$ and $R_{on}Q_{gd}$, respectively, Table 1 and Figure 2). The reduced capacitance/charge compensated for the increased $R_{on,sp}$ (measured at 20V gate potential, 10A drain current) of the OCTFET layout, relative to linear cells.

Low C_{gd} also boosted the C_{iss}/C_{gd} FOM, where C_{iss} is the input capacitance, i.e. the sum of C_{gd} and C_{gs} . Large values of the C_{iss}/C_{gd} FOM are associated with false-turn-on suppression and low shoot-through current

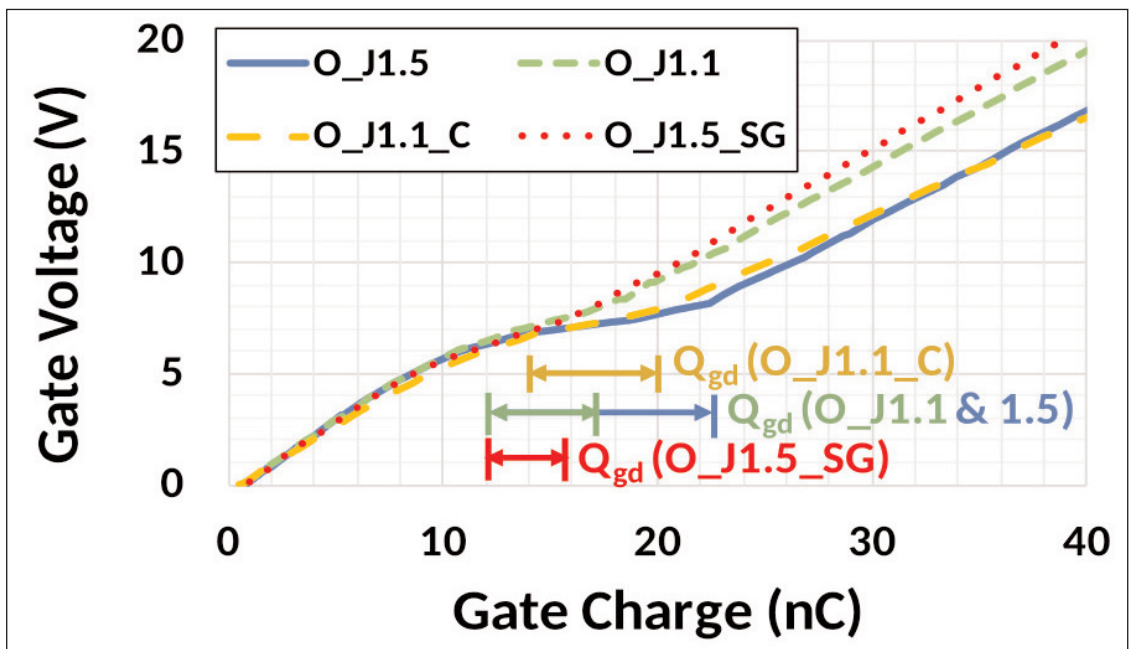


Figure 2. Measured gate charge of fabricated OCTFETs and SG-OCTFET at 800V drain bias and 10A drain current. Active area 0.045cm².

when the voltage changes rapidly. The output capacitance, C_{oss} , is the sum of C_{ds} and C_{gd} .

Han and Baliga also quote the RQ FOM values for Infineon's silicon-based 600V COOLMOS power transistor (IPL60R365P7) at 1240 (310m Ω x4nC), and Cree's 'state-of-the-art' 1.2kV SiC power linear cell topology MOSFET (CREE C2M0160120D) at 2240 (160m Ω x14nC). The researchers write: "Our work demonstrates for the first time that a HF-FOM [$R_{on} \times Q_{gd}$] 1.66-times better than the 600V COOLMOS product can be achieved in a 1.2kV SiC power MOSFET by using the SG-OCTFET topology, which opens new application opportunities for 1.2kV SiC power MOSFETs." ■

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Table 1. Experimental results for OCTFETs and split-gate OCFET with varying dimensions: O_J1.5,

	O_J1.5	O_J1.1	O_J1.1_C	O_J1.5_SG
WA-A'	5.10 μ m	4.53 μ m	3.75 μ m	5.10 μ m
Channel density	0.256/ μ m	0.259/ μ m	0.377/ μ m	0.256/ μ m
JFET (X) density	0.144	0.098	0.143	0.052
Breakdown	1607V	1605V	1605V	1625V
V _{th}	2.12V	2.02V	2.12V	2.02V
R _{on,sp}	8.38m Ω -cm ²	12.82m Ω -cm ²	8.47m Ω -cm ²	8.51m Ω -cm ²
C _{iss,sp}	32nF/cm ²	33nF/cm ²	37nF/cm ²	33nF/cm ²
C _{oss,sp}	1073pF/cm ²	1067pF/cm ²	1069pF/cm ²	1076pF/cm ²
C _{gd,sp}	62pF/cm ²	35pF/cm ²	48pF/cm ²	27pF/cm ²
Q _{gd,sp}	233nC/cm ²	113nC/cm ²	144nC/cm ²	88nC/cm ²
C _{iss} /C _{gd} FOM	516	943	771	1222
R _{on} x C _{gd} HF-FOM	520m Ω -pF	449m Ω -pF	407m Ω -pF	230m Ω -pF
R _{on} x Q _{gd} HF-FOM	1953m Ω -nC	1449m Ω -nC	1220m Ω -nC	749m Ω -nC