Reaching new heights by producing 1200V SiC MOSFETs in CMOS fab

Monolith Semiconductor and Littelfuse describe how 1200V silicon carbide MOSFETs can be mass produced on 150mm wafers in a CMOS silicon fab.

The emergence of silicon carbide (SiC) power devices has brought the advantages of high-speed unipolar devices into much higher-voltage classes than would be achievable with silicon devices. SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) demonstrate dramatically lower switching losses than similarly rated silicon IGBTs.

The very first commercial SiC MOSFETs rated at 1200V were introduced to the market back in January 2011 [1]. Since then, a growing number of power electronics systems manufacturers have turned to subsequent generations of these devices in order to achieve greater efficiency, power density, and reliability at a lower cost. However, in order for these devices to reach their commercial potential, providing a high-performance, near-ideal switch is not enough to ensure the widespread adoption of these devices. SiC MOSFET manufacturers also must be able to offer their power electronics customers' devices that combine good manufacturability, long-term reliability, and exceptional ruggedness, all at a competitive price (Figure 1).

One approach to reaching this goal is to move from 76mm (3-inch)- and 100mm (4-inch)-diameter SiC wafers to 150mm (6-inch) SiC wafers and develop design and process techniques that are compatible with processes in a CMOS fab. Integrating the process flows for both silicon and SiC wafers and running them in parallel allows one to take advantage of enormous economies of scale. The results of this approach, employed recently in the production of 1200V SiC MOSFETs in an automotive-qualified 150mm CMOS fab, have demonstrated not only high manufacturability but also superior device performance, gate oxide reliability and robustness at operating junction temperatures of 175ºC.

Figure 1. Widespread adoption of high-voltage SiC MOSFETs will require much more than just high-performance devices.

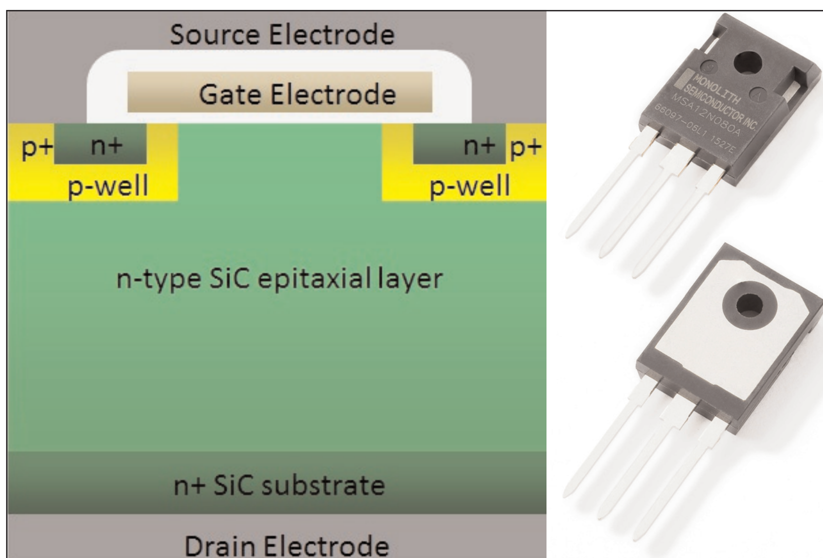

Figure 2. Cross section of a planar SiC MOSFET. Proper design of a MOSFET with planar structure ensures the device is rugged and reliable. The SiC MOSFET packaged in an industry-standard TO-247 package.

Silicon carbide fabrication processes and device design

More than 90% of SiC device processes are compatible with processes already in use in silicon CMOS fabs. Although the nature of SiC as a material makes it fundamentally compatible with most CMOS fab processes, significant hurdles remain before this approach can be realized, including requirements for high-temperature processing. Other challenges include integrating CMOS- and SiC-specific process steps, as well as making metal and dielectric stacks used in the SiC MOSFET compatible with a conventional CMOS fab. Whenever possible, standard process steps available in a CMOS foundry should be reused with SiC wafers, such as implantation masks and top-level interconnects.

For steps such as gate oxidation and metallization, SiC-specific processes can be developed using CMOS production tools like high-temperature furnaces and rapid thermal processing (RTP) ovens, but dedicated tools are required for implant activation and certain ion implantation steps. It's also necessary to modify the mechanical wafer handling methods used because of the semi-transparent nature of SiC wafers. For example, sensors set up for use with opaque materials will respond incorrectly when used with SiC wafers, leading to wafer breakage during loading/unloading .Similarly, automated defect detection tools can confuse sub-surface features with surface defects. Differences in wafer thickness can also complicate wafer handling. Nevertheless, with the proper process modifications, SiC and silicon wafers can be run in parallel in a high-volume production environment, taking advantage of the economies of scale associated with the production processes already in place in the CMOS fab.

Producing rugged SiC MOSFETs (see Figure 2) with wide process margins demands ensuring stable and uniform avalanche breakdown in the device unit cells, avoiding high fields in the oxide, and breakdown in the edge termination. Ideally, device termination should achieve close-to-ideal parallel plane breakdown voltage over a broad dose range, providing a wide process margin.

In addition to the device termination, the JFET region of the device under oxide must be optimized with appropriate doping concentration and physical dimensions. Figure 3 illustrates an example of impact ionization contours at device breakdown. In this case, the device was designed to preferentially break down at the center of the unit cell, ensuring uniform avalanche conditions and a low peak field in the oxide. Other critical aspects of the device and process design included optimization of the channel and P-well designs to ensure the device remained off over the entire voltage and temperature envelope.

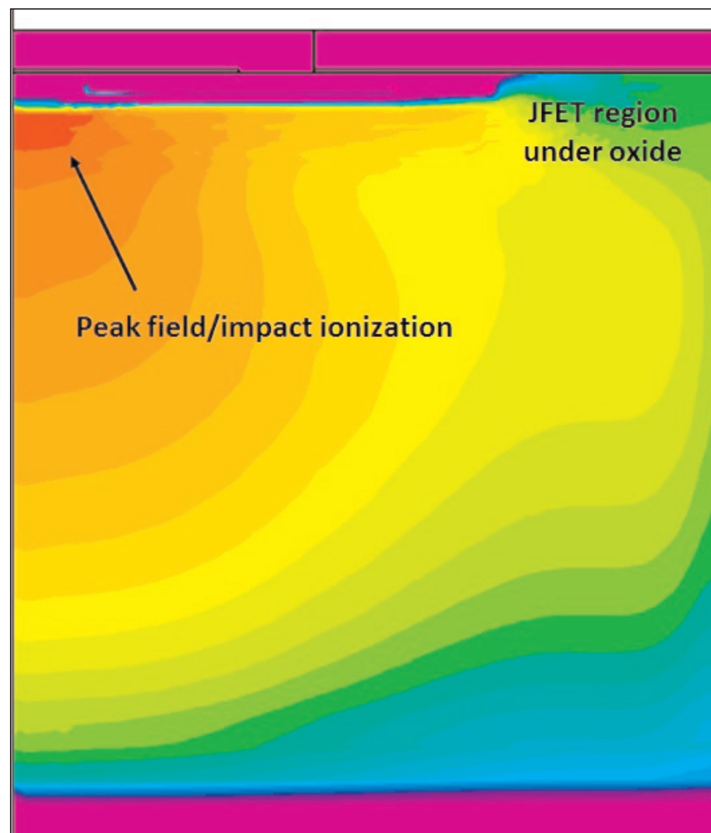

Figure 3. Impact ionization contours at device breakdown. The device was designed to break down at the center of the unit cell, ensuring stable avalanche breakdown.

Performance of fabricated devices

Figure 4 shows a fully processed 150mm SiC wafer with 1.2kV, 65mΩ MOSFETs fabricated in an automotive-qualified fab using the process outlined in this article. Multiple wafer lots have been produced with various process and design splits. The devices produced have been thoroughly characterized at both the wafer level and in TO-247 packages. Wafer-level results have been used to generate wafer maps and gain an understanding of various process-design interactions. Packaged parts are used for final reliability and ruggedness evaluations.

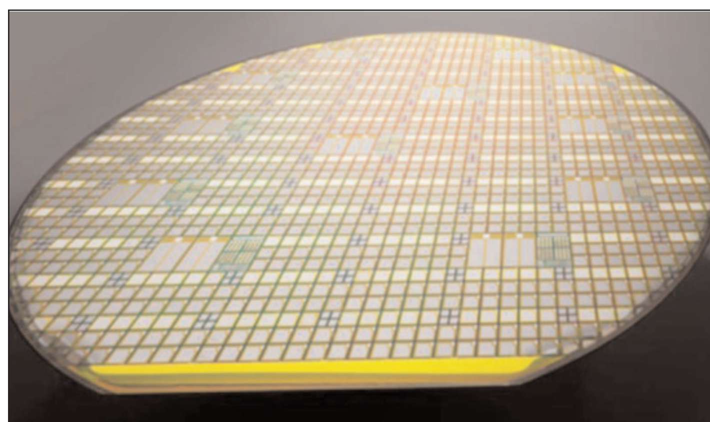

Figure 4. Fully processed 150mm SiC wafer with 1.2kV MOSFETs and process control monitors.

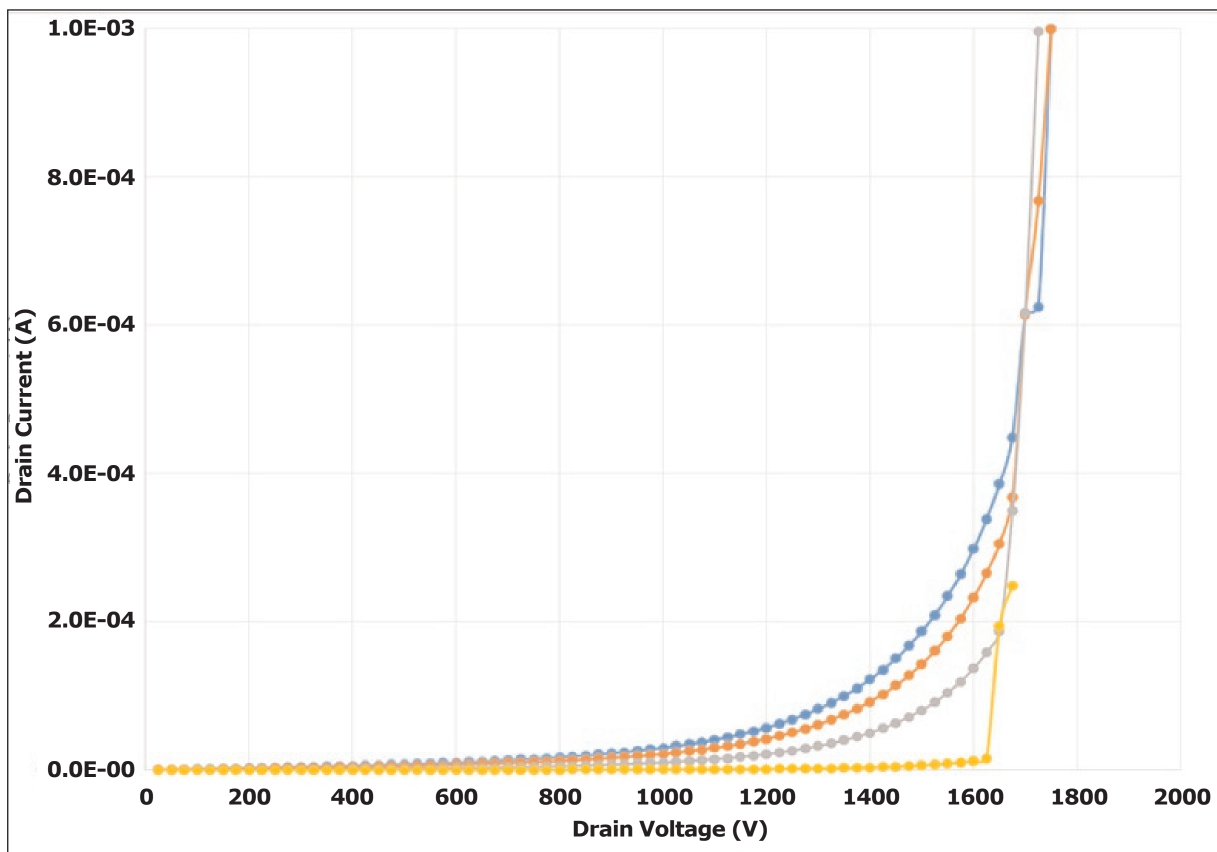

Figure 5. Typical forward characteristics (I_{DSS}; V_{GS} = 0) of manufactured MOSFETs for temperatures from 25ºC to 175ºC. Results show low leakage current up to 1200V and 175ºC.

Figure 5 presents the typical off-state IV (V_{GS} = 0) characteristics of the fabricated MOSFETs from 25ºC to 175ºC with low leakage current (<100μA) over a worst-case voltage and temperature envelope.

Figure 6 compares the forward characteristics of these devices at 25ºC and 175ºC. The typical on-resistance of these MOSFETs at V_{GS} = 20V, 25ºC is 65mΩ. Although these devices were optimized for robustness and manufacturability, the typical specific on-resistance R_{sp} (normalized to the devices' active area) is competitive with that of other commercially available 1200V SiC MOSFETs. With more aggressive processes and designs, it has proven possible to achieve R_{sp} of 3.1mΩ-cm^2 on an identical process platform.

Figure 7 details the SiC MOSFET's low switching losses when characterized at 800V, 20A. Switching loss at a gate resistance of 4.8Ω was under 400μJ, indicating superior switching performance.

Evaluating device manufacturability

Controlling SiC MOSFET production costs effectively demands a highly manufacturable process with sufficient margin. To evaluate the manufacturability of this process, we analyzed the breakdown voltage distribution of a

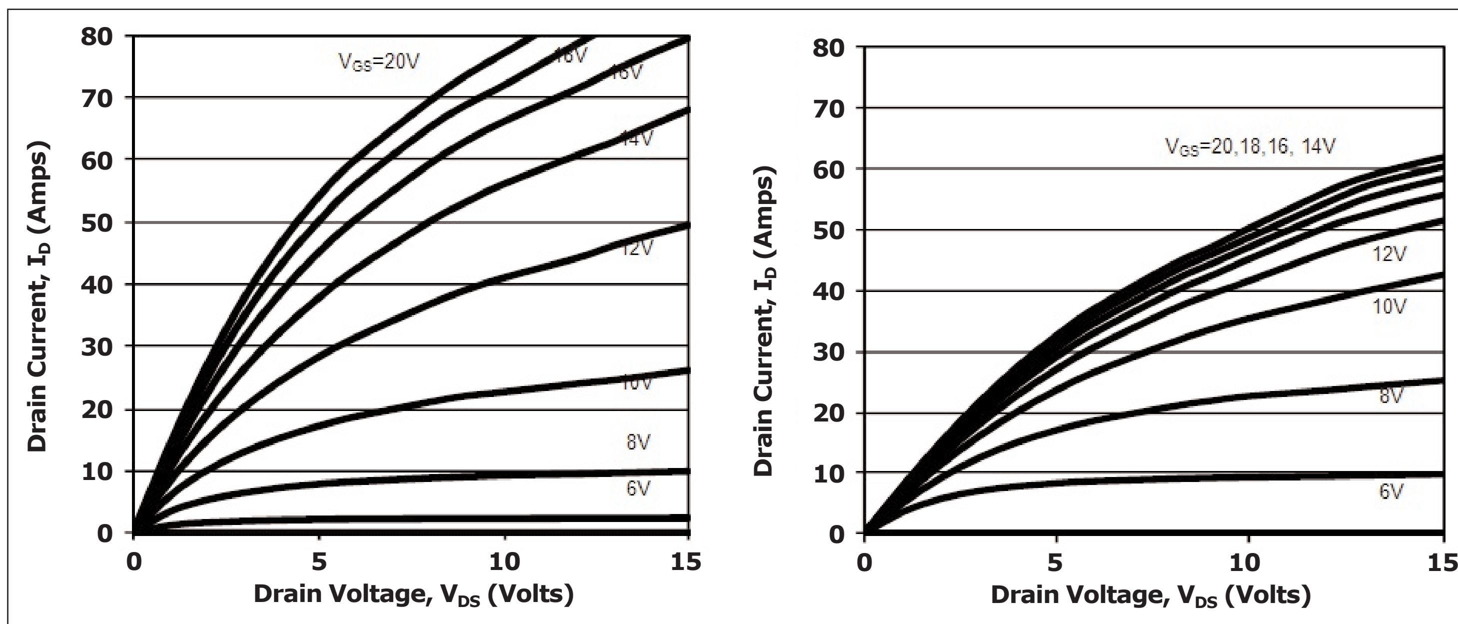

Figure 6. Forward characteristics at 25ºC (left) and 175ºC (right).

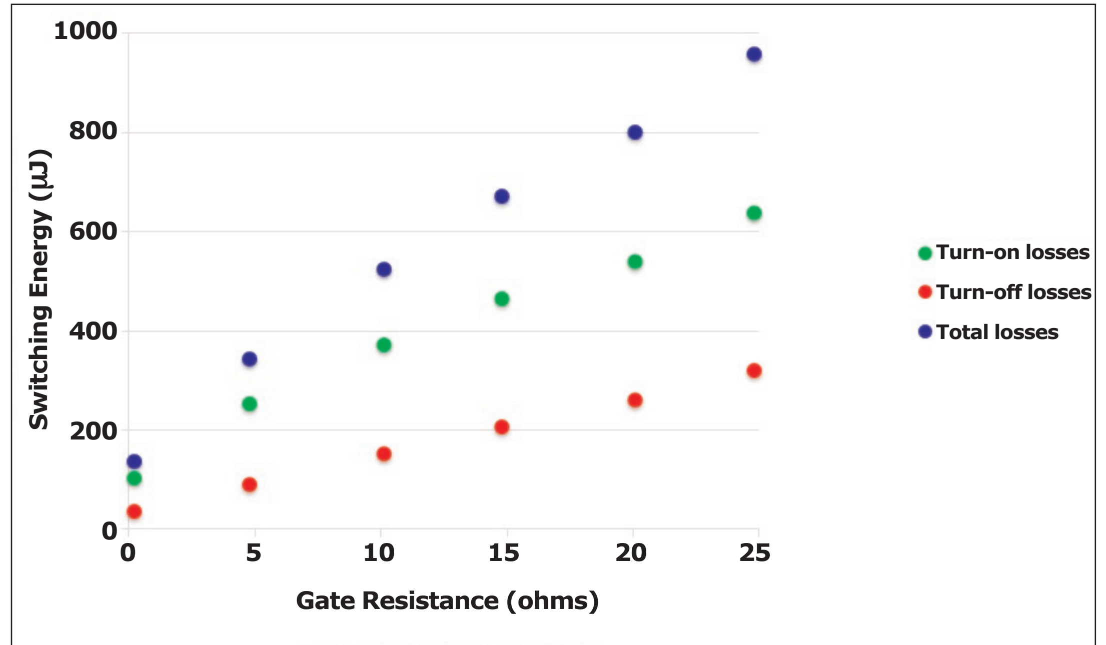

Figure 7. The devices exhibited less than 400μJ of switching loss at a gate resistance of 4.8Ω.

large quantity of devices from multiple wafers from different fab lots (Figure 8). This analysis showed that the process offers sufficient margin to accommodate a wide range of epilayer doping variations.

As part of our manufacturability analysis, we also analyzed $R_{DS(on)}$ or on-resistance (Figure 9). Note that the on-resistance distribution is quite tight despite the epitaxial layer doping variation.

Given that 150mm SiC wafers are not yet as common as 100mm SiC wafers, the diode leakage current of the fabricated devices was also investigated to assess defect density and device yields. Diode leakage wafer maps revealed only randomly located failures and >90% yields, which eliminated any concerns about the quality of 150mm wafers affecting device yields. Work on improving the epitaxial doping control aspect of the process continues. Doping variation has been taken into account in these designs and it is reflected in the wide breakdown voltage margin.

Assessing device ruggedness and reliability

A number of techniques were used to evaluate the ruggedness of the devices produced, including the avalanche energy of the device. Figure 10 shows the typical waveform from avalanche energy characterization of the device with an avalanche energy >1 Joule.

Because gate oxide quality is a common concern for SiC MOSFETs, the fundamental quality of the gate oxide process was studied previously using time-dependent dielectric breakdown (TDDB) measurement of capacitors at high temperatures [2]. Charge-to-breakdown (Q_{BD}) measurements in large-area DMOSFETs produced Q_{BD} values that were well above $10C/cm^2$ (see Figure 11) and no defective tail that would indicate intrinsic failure modes. High-temperature gate bias (HTGB) testing at V_{GS} of −10V and +20V showed excellent stability of threshold voltage, as presented in [3]. The MOSFETs were also subjected to 1400 hours of high-temperature (175ºC) reverse bias (HTRB) testing at V_{DS} = 960V and V_{GS} = 0V, and stable breakdown voltage characteristics were observed.

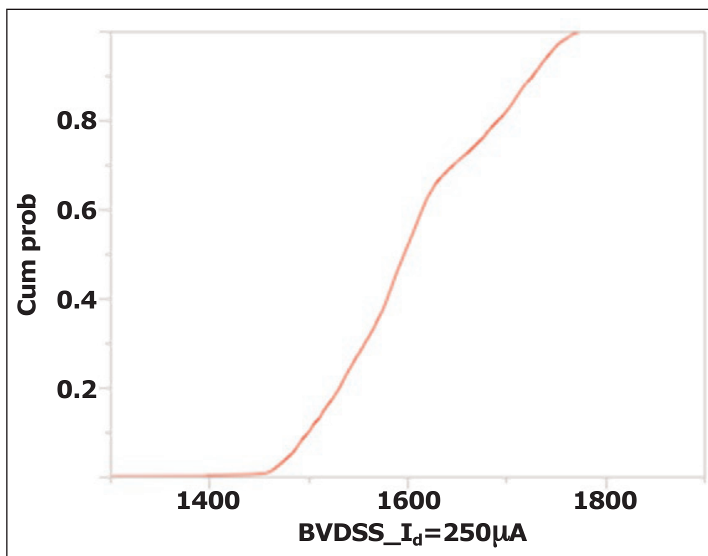

Figure 8. Breakdown voltage distribution of a large quantity of devices from multiple wafers from different fab lots.

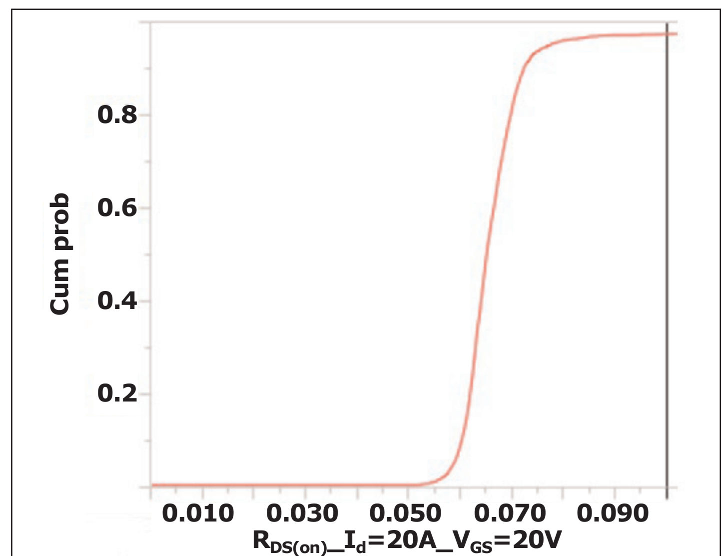

Figure 9. On-resistance distribution of a large quantity of devices from multiple wafers from different fab lots.

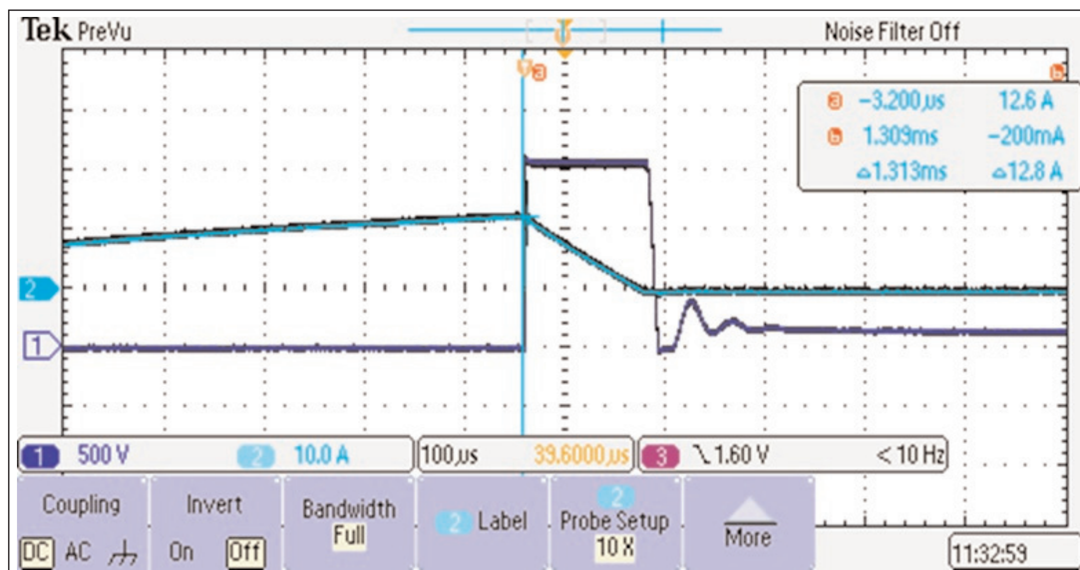

Figure 10. Avalanche energy characterization of the SiC MOSFETs, showing avalanche energy > 1 Joule.

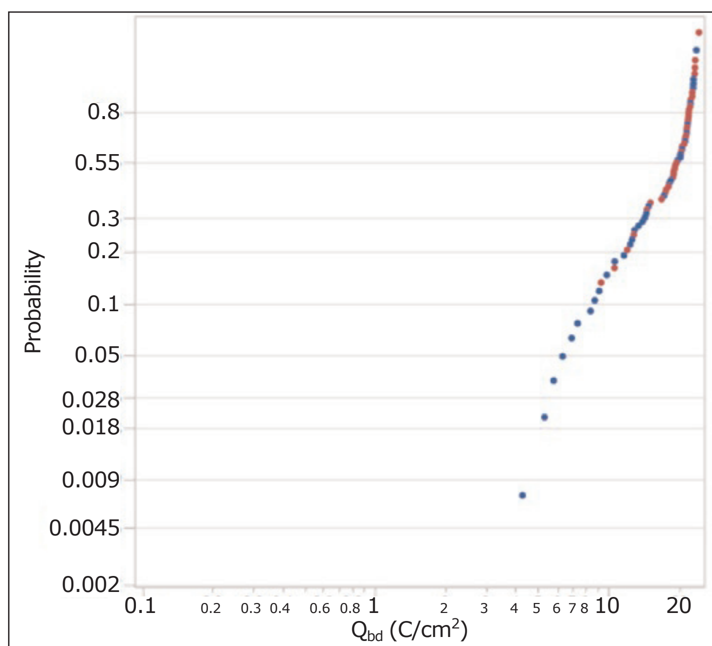

Figure 11. Results of charge-to-breakdown (Q_{BD}) measurements in large-area DMOSFETs.

Conclusion

In the coming years, the average selling price of commercial 1200V SiC MOSFETS is likely to continue to decrease, from the present price of ~50 cents/amp to somewhere around 10 cents/amp by the end of the decade. However, in order to achieve this price point and allow for widespread adoption of SiC power MOSFETs, suppliers must continue to explore opportunities to lower their costs without compromising device quality. Producing these devices in high-volume, automotive-qualified 150mm CMOS fabs has proven to be one way to achieve this goal [4]. ■

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