Pushing forward with compound semiconductor technologies

Mike Cooke reports on research presented at the Symposium on VLSI Technology.

The development of III–V devices is progressing rapidly, with many new achievements and records reported by research groups at the 2017 Symposium on VLSI Technology and Circuits in Kyoto, Japan (5–9 June). Most of the reported work involved indium gallium arsenide (InGaAs), particularly integrated with silicon (Si) substrates aiming for low-cost mass production. We report here on those sessions, along with research aimed at gallium nitride (GaN) devices for high-power switching applications.

Transistor/laser integration on silicon

The National University of Singapore (NUS), Nanyang Technological University (NTU) in Singapore and Massachusetts Institute of Technology (MIT) in the USA claim the first monolithic integration of InGaAs field-effect transistors (FETs) and gallium arsenide/aluminium gallium arsenide (GaAs/AlGaAs) quantum well (QW) laser diodes (LDs) on silicon substrate through direct epitaxial growth [Session T5-2].

The researchers targeted a low sub-400ºC thermal budget process and see the achievement as a milestone towards enabling low-power and high-speed complex optoelectronic integrated circuits. On-chip and inter-chip optical communications would enable low-power and high-bandwidth computer and data transmission systems.

Molecular beam epitaxy (MBE) was used to grow III–V material on a 6º-offcut Ge-on-Si (100) substrate (Figure 1).

Laser structures contained graded-index separate-confinement heterostructure AlGaAs, with the aluminium content varying between 30% and 60%. The graded material bridged between 1mm $Al_{0.6}Ga_{0.4}As$ cladding and $Al_{0.3}Ga_{0.7}As$ barriers in which a single GaAs quantum well formed the active light emitter for the laser.

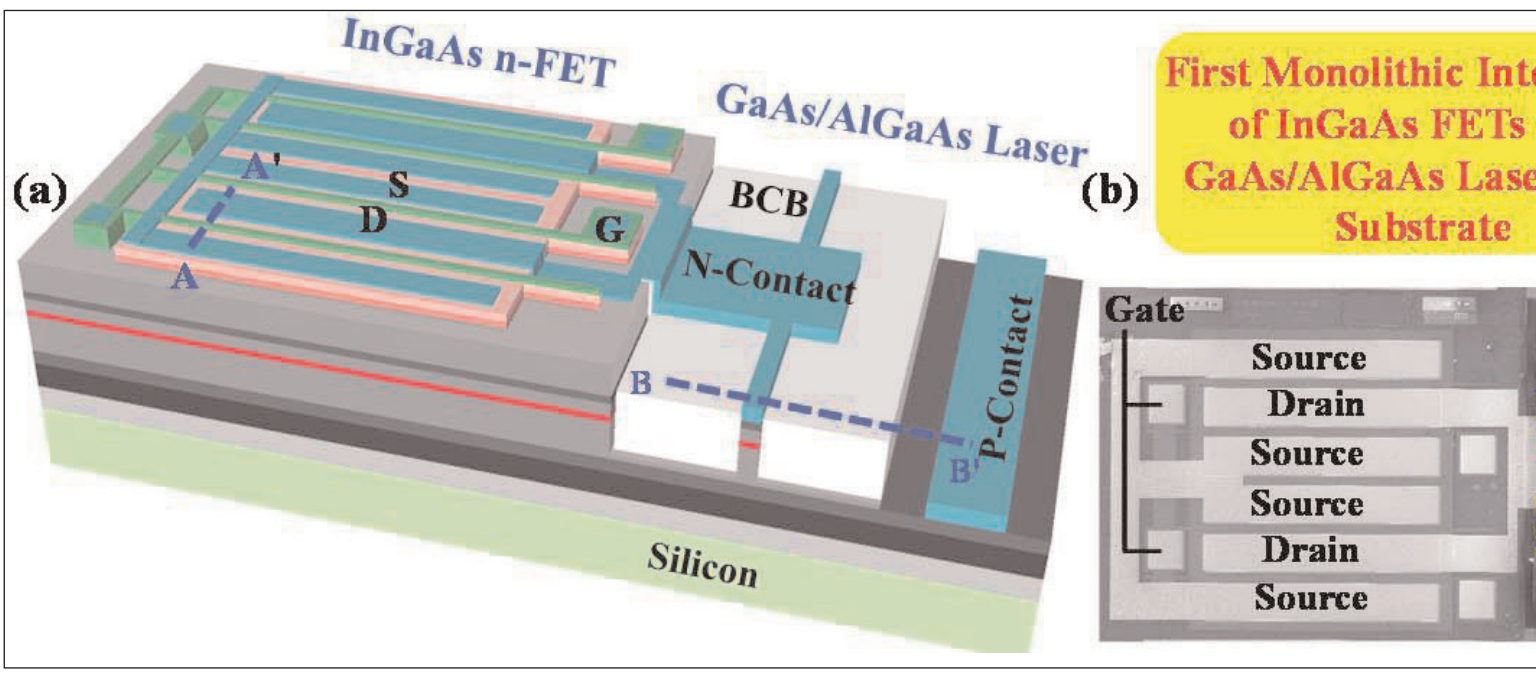


Figure 1. (a) Three-dimensional schematic of monolithic integration of InGaAs n-FETs with lasers on silicon substra finger InGaAs FETs driving laser. (c) Cross-sectional schematic along A–A' in (a). (d) Cross-sectional schematic alo

Transistor layers were grown on top of the laser structure: 800nm InAlAs graded buffer (indium content 10–52%), 15nm $In_{0.53}Ga_{0.47}As$ channel, 1nm $In_{0.52}Al_{0.48}As$ etch stop, and 25nm n^+-$In_{0.53}Ga_{0.47}As$ cap.

FET fabrication began with the blanket metal deposition of tungsten (W) and molybdenum (Mo). Fluorine-based reactive ion etch removed metal from the channel region. Wet etch removed III–V material down to the InAlAs etch-stop layer. The gate insulator consisted of atomic layer deposition (ALD) 2nm/5nm aluminium oxide/hafnium dioxide (Al_2O_3/HfO_2). The gate metals were then deposited and etched. The devices were completed with wet etch to give mesa device isolation.

Plasma-enhanced chemical vapor deposition (PECVD) silicon dioxide (SiO_2) was used as a mask for etching the laser region. Wet etch was used to form the waveguide, and then dry etch formed the vertical/smooth laser facets. Surfaces were passivated with benzocyclobutene (BCB) before deposition of the metal contacts and interconnects.

A 500nm-channel-length n-FET achieved an on/off current ratio of 10^6 and subthreshold swing of 83mV/decade. The current was 400μA/μm with 1.5V drain bias and 1.5V overdrive (gate potential above threshold). The source-drain resistance is described as being large (~1.8kΩ-μm).

The subthreshold swing (SS) reduced to 75mV/decade after laser diode fabrication. The researchers explain: "This indicates excellent electrostatic gate control and gate stack quality of the InGaAs n-FETs. Improvement in subthreshold swing after laser diode fabrication is attributed to the reduction of interface traps at Al_2O_3/InGaAs interface during SiO_2 deposition at 350ºC using PECVD."

Laser diode fabrication also reduced the spread in threshold voltage. The team comments: "This positive shift in V_T can be explained by reduction of fixed positive charges in high-k layer during SiO_2 deposition at 350ºC."

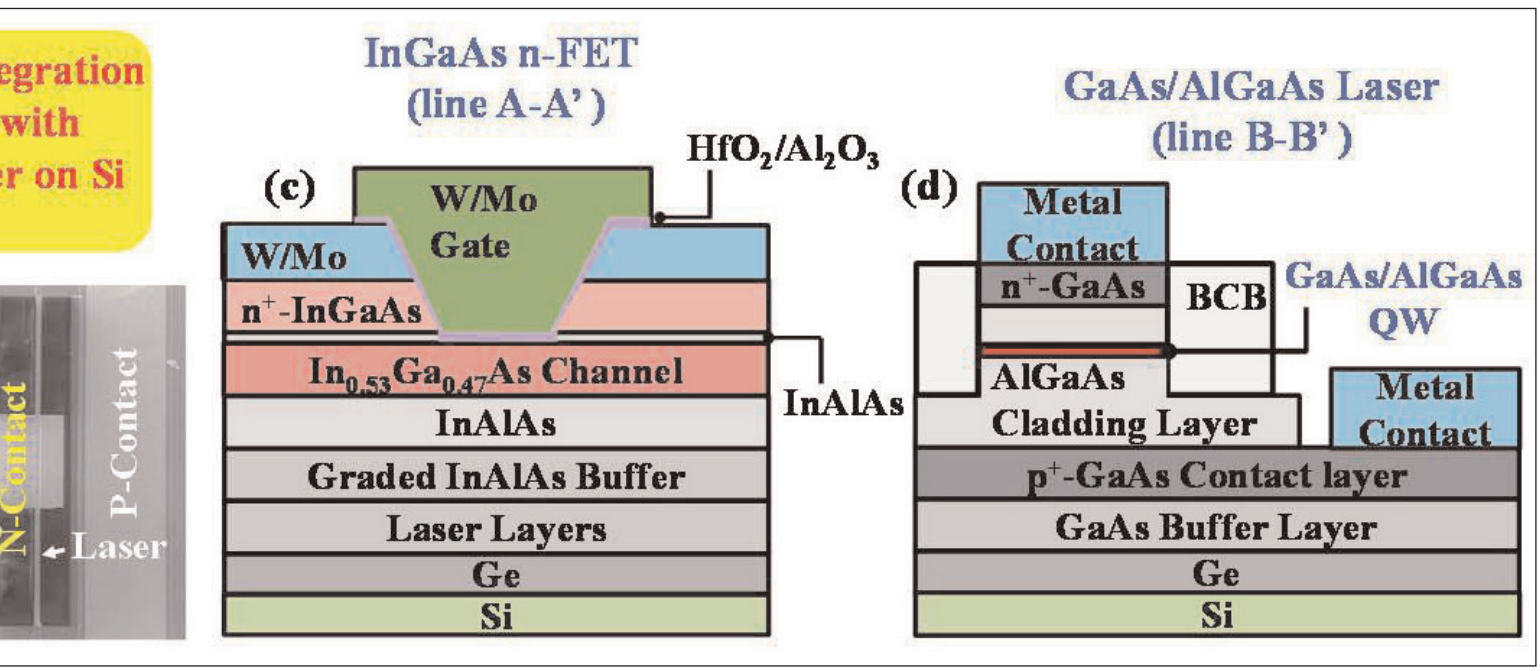
The peak effective mobility was 1920cm^2/V-s.

The laser diode had an on/off current ratio of 10^3. Threshold at 5ºC came at ~5kA/cm^2 pulsed current density with ~790nm wavelength. Above threshold, the linewidth reduced to less than 0.5nm The output power dropped with increasing temperature. The researchers also showed successful modulation of laser diode voltage and injection current by varying the FET's gate voltage.

InGaAs FETs

Lund University in Sweden reports the achievement of record on-current and optimal transconductance and subthreshold swing for vertical metal-oxide-semiconductor FETs (MOSFETs) [Session T3-2]. The researchers point out that vertical MOSFETs could give advantages over the traditional planar devices at the 5nm node. The vertical format decouples device area from gate length scaling. Off current is reduced by restricting substrate leakage.

The n^+-InAs source contact layer of the FETs was grown on silicon by metal-organic vapor phase epitaxy (MOVPE). The nanowires were defined by gold particles that formed the seed of vapor-liquid-solid growth. The core diameter corresponded to that of the gold seed. The nanowire was covered by a ~5nm shell of InGaAs.



te. (b) Top-view scanning electron microscope (SEM) image of optoelectronic integrated circuit with multiple-ng B–B' in (a).

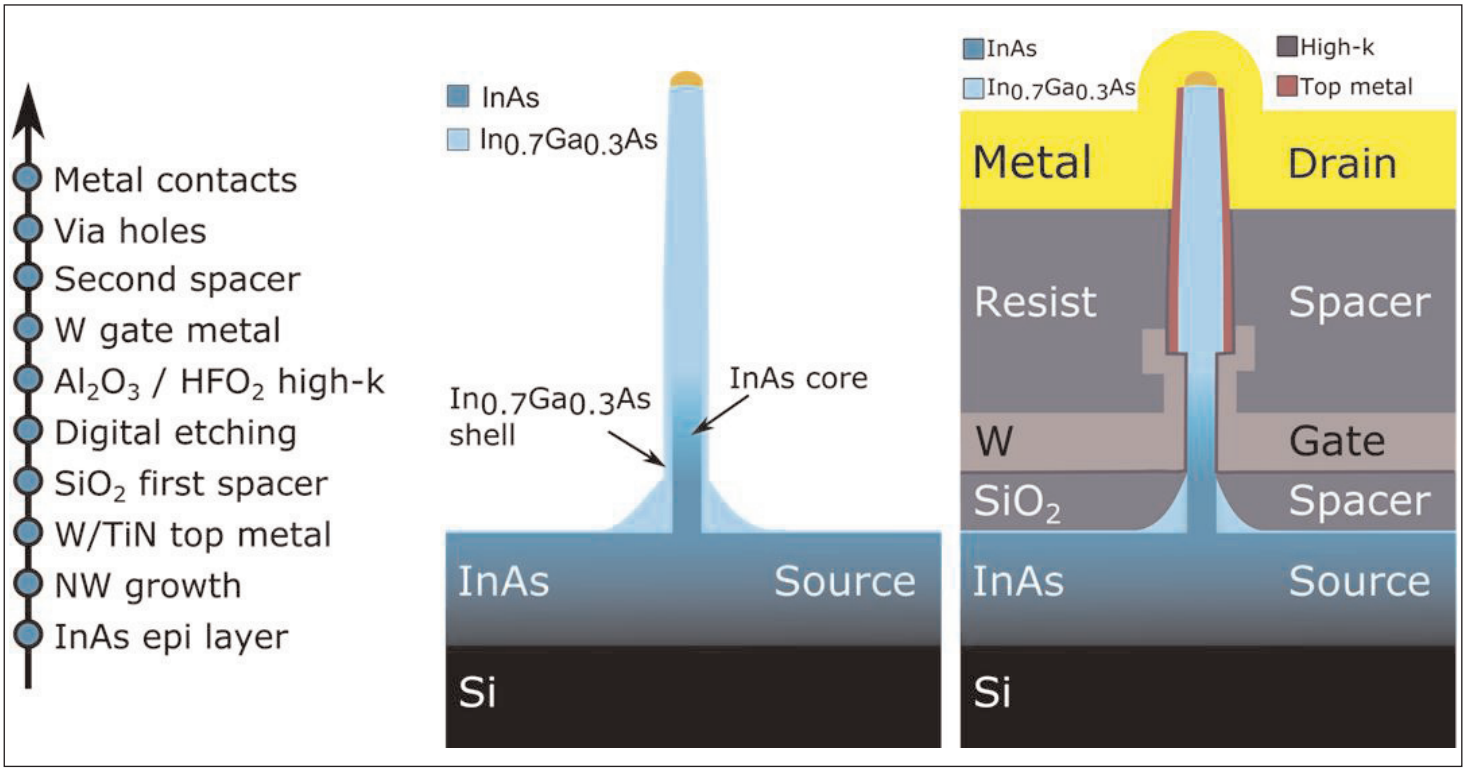


Figure 2. Illustrations of process flow (a), cross-section schematic of device after growth (b), cross-sectional schematic of finalized device (c) and SEM of the completed device.

The transistors were fabricated with a self-aligned gate-last process with the aim of reduced access resistance (Figure 2). Tungsten and titanium nitride (W/TiN) were used for the top metal. Digital etching of the channel region was achieved using ozone oxidation and hydrochloric acid wet steps to remove the shell layers. The Al_2O_3/HfO_2 gate insulator had an equivalent oxide thickness (EOT) of 1.5nm.

A device with 260nm channel length (160nm effective with contact overlap) and 28nm diameter had a peak transconductance (g_m) of 1.4mS/μm and SS of 85mV/decade with 330μA/μm on-current and 100nA/μm off-current at 0.5V drain. The researchers claim records for the on-current and Q-factor (g_m/SS) of 16 (1400/85). A lower off-current of 1nA/μm corresponded with a somewhat lower on-current of 46μA\μm at 0.5V drain.

"This is the first demonstration of a non-planar, III–V MOSFET on Si achieving I_{off} = 1nA/μm," the team adds.

A lower SS of 68mV/decade was achieved with an effective channel length of 145nm and 35nm diameter. The g_m was 0.58mS/μm. On-currents of 170μA/μm and 88μA/μm corresponded to 100nA/μm and 1nA/μm, respectively.

"Our devices show clear improvement compared to vertical MOSFETs, although state-of-the-art planar/lateral MOSFETs still have higher I_{on}," the researchers

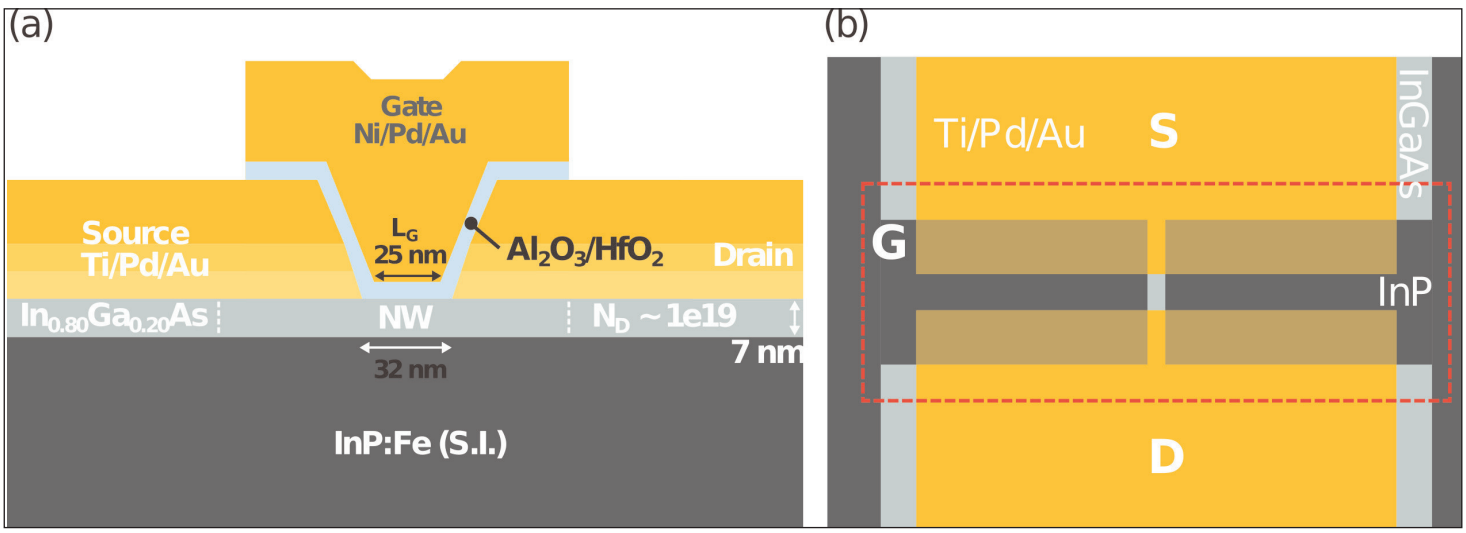


Figure 3. Schematic figures of single-layer junctionless device in (a) side and (b) top views.

report. The barrier to higher on-current seems to be high contact resistance in the vertical devices.

Another group from Sweden's Lund University claims record performance for junctionless field-effect transistors (JLFETs) based on InGaAs nanowires (NWs) [Session T3-1]. Junctionless transistors have uniform high doping in the channel region without oppositely doped source/drain regions, avoiding re-growth or implantation processes.

Nanowires were grown by metal-organic chemical vapor deposition (MOCVD) on semi-insulating iron-doped indium phosphide (Figure 3). A hydrogen silsesquioxane (HSQ) mask was used for selective area growth of the 14nm-high n-$In_{0.2}Ga_{0.8}As$ nanowires.

Etching was carried out to create 700nm-wide device mesas. The InGaAs height was reduced to 7nm by a digital etch. The etch also reduced the NW width by 14nm. Source/drain electrodes were deposited, followed by 1nm/4nm Al_2O_3/HfO_2 gate oxide. The effective gate length was 25nm.

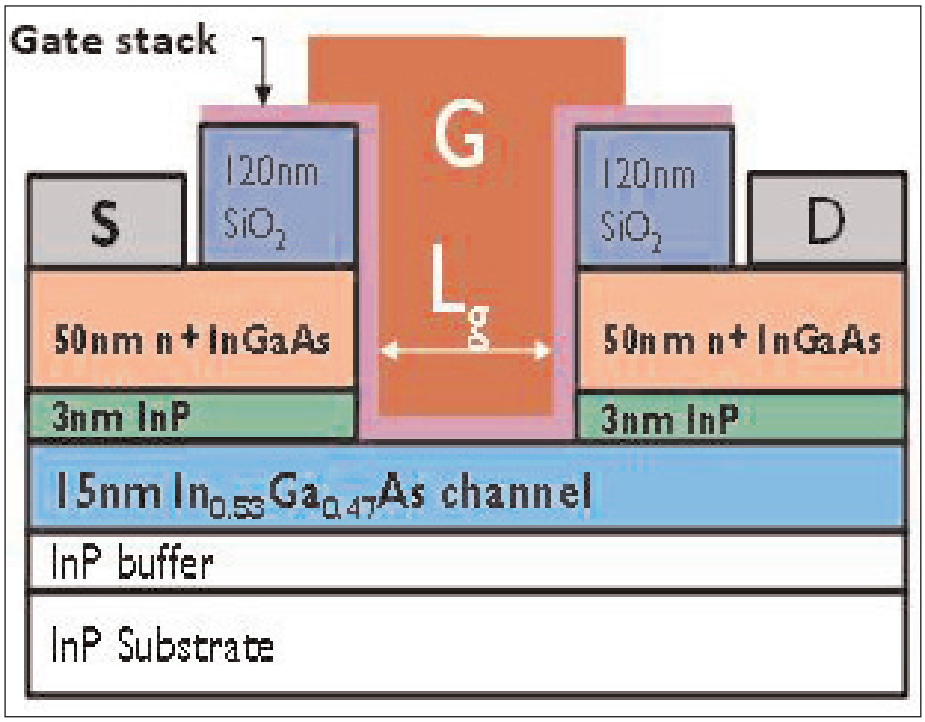


Figure 4. Implant-free InGaAs n-MOSFET.

Devices with 16nm NW width had low subthreshold swing of 76mV/decade and drain-induced barrier lowering (DIBL) of 33mV/V. A drain current of 160μA/μm (220μA/μm normalized according to chip surface width) is claimed as a record for JLFETs. The drain bias was 0.5V and the off-current was 100nA/μm. With a lower off-current of 10nA/μm, the on-current was 80μA/μm, also claimed as a record for JLFETs. The SS increased with NW width to 120mV/decade for 60nm.

The researchers also claim the peak transconductance of 1.6mS/μm at 0.5V drain as a JLFET record. The team reports that performance is presently limited by access resistance from the thin contacts, rather than degradation of electron mobility in the doped channel.

IMEC in Belgium claims the first demonstration of implant-free $In_{0.53}Ga_{0.47}As$ n-MOSFETs meeting reliability targets for advanced technology nodes of maximum overdrive voltage (gate-threshold) of 0.6V with equivalent oxide thickness (EOT) of 1.15nm [Session T3-3]. Key to the development was a new gate insulation structure with an unspecified interlayer (IL), lanthanum silicon oxide ($LaSiO_x$) and HfO_2. One suspects that the interlayer is being kept secret so that collaborators from the Belgium and USA sections of toolmaker ASM can help their company gain competitive advantage.

The researchers also claim record mobility of 3531cm^2/V-s and low SS (71mV/decade) at 1.15nm EOT.

The MOSFET III–V layers were grown on 2-inch semi-insulating InP (Figure 4). The gate-insulation structure of 1nm/1nm/3nm interlayer/$LaSiO_x/HfO_2$ was compared with various alternatives — IL/Al_2O_3/HfO_2 (1nm/1nm/3nm), $LaSiO_x/HfO_2$ (1nm/3nm), and IL/HfO_2 (1nm/3nm). The gate metal was titanium nitride (TiN). The gate insulator was applied using atomic layer deposition.

Capacitance–voltage measurements showed reduced interface trap density and capacitive equivalent thickness (CET) of the IL/$LaSiO_x/HfO_2$ gate stack. The CET was 1.55nm and equivalent oxide thickness was 1.15nm. Oxide charge traps were reduced to ~$10^{10}/cm^2$ for 3.5MV/cm field — "meeting the target for 10 years operation", according to the IMEC team.

Time-of-flight secondary-ion mass spectrometry suggested that the $LaSiO_x$ stabilizes the underlying interlayer, limiting diffusion down into the substrate.

Reducing the HfO_2 layer of the new gate stack to 2nm gave a CET of 1.46nm and an EOT of 1.06nm. This allowed the reduction of subthreshold swing to 68mV/decade.

The team comments: "As the processing of this gate stack is ALD based, it shows high potential for transfer to advanced device architectures such as horizontal and vertical nanowires."

Three-dimensional monolithic (3DM) integration of InGaAs n-FETs on fully depleted silicon-on-insulator (FDSOI) complementary MOS (CMOS) has been achieved by IBM Research GmbH Zürich Laboratory in Switzerland and CEA-Leti, MINATEC Campus, in France [Session T6-4]. A benefit of the 3DM approach is it allows specific processes with different thermal budgets to be carried out.

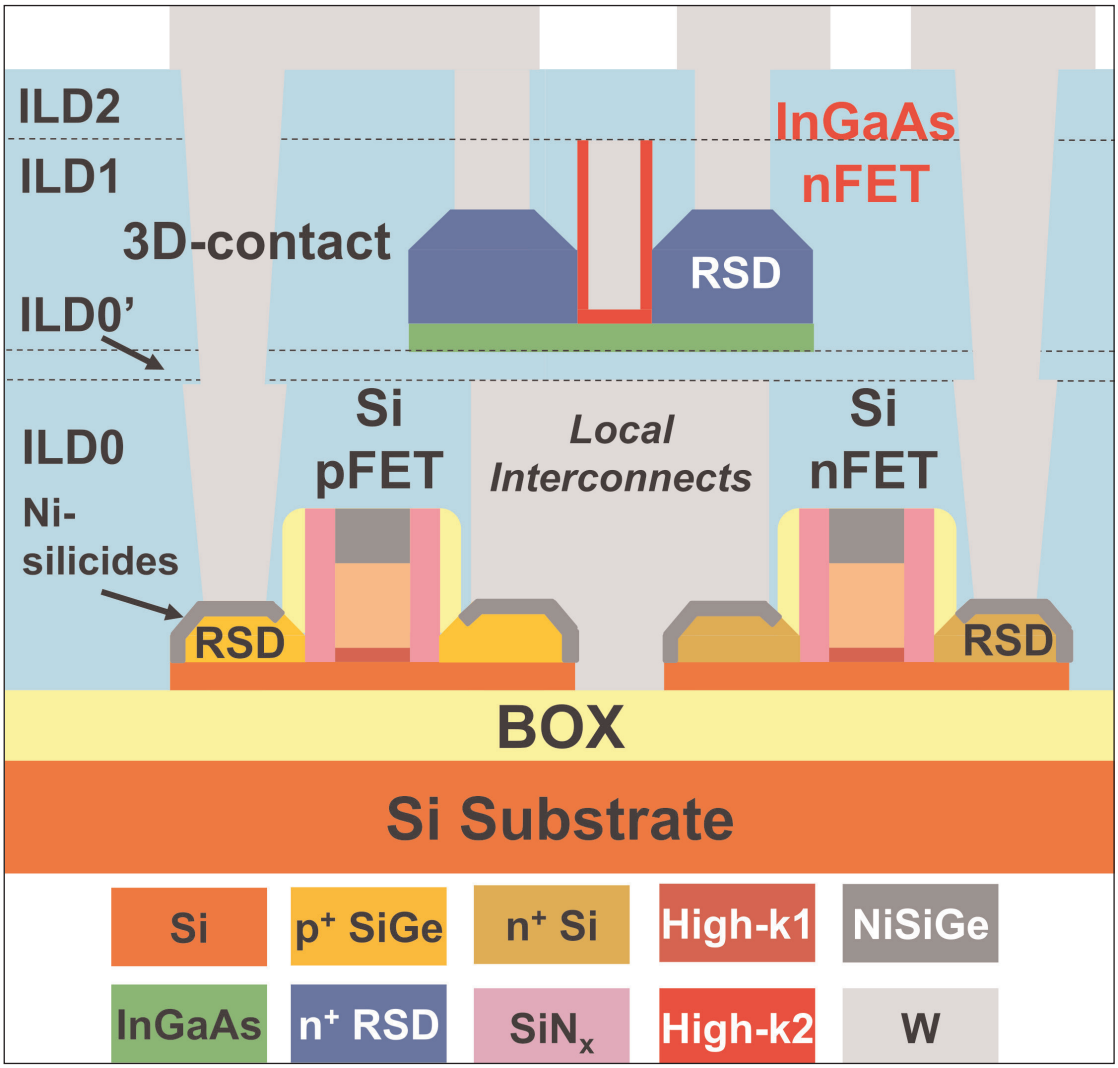


Figure 5. Schematic showing 3D monolithic stack of RMG InGaAs n-FET layer on FDSOI silicon CMOS layer.

The structure (Figure 5) combined a replacement metal gate (RMG) InGaAs n-FET and fully depleted SOI CMOS. The ~20nm InGaAs material was transferred to the SOI CMOS structure by direct wafer bonding on a thin interlayer dielectric (ILD0') before fabrication of the InGaAs n-FET. InGaAs n-FET devices managed ~70mV/decade SS down to 25nm gate length.

The researchers used the technology to fabricate 6-transistor SRAM circuits with 60nm-gate InGaAs n-FETs and 30nm-gate Si p-finFETs. "This is the first demonstration of a hybrid 3D 6T-SRAM utilizing 3DM integration of InGaAs nFETs over Si CMOS," the researchers claim. The team also says that its technology offers denser packing compared with 2D layouts. Apart from dense digital circuits, the researchers believe that functional integration of RF-on-Si could be forthcoming.

IBM T. J. Watson Research Center in the USA and Samsung and its Texas-based Advanced Logic Lab have used aspect ratio trapping (ART) to reduce defects in InGaAs buffers grown on silicon [Session T3-4]. An optimized ART process reduced junction leakage by six orders of magnitude. The fabrication of FinFETs used a gate-first process.

The device structure avoided parasitic bipolar effects (PBEs) that have been seen in III–V on insulator transistors. PBEs amplify leakage current due to the accumulation of holes injected by band-to-band tunneling at the drain end of the n-FET through a bipolar junction transistor action. Also, the researchers successfully thinned the fins to 9nm, improving short-channel control.

Using a drain bias of 0.5V and fixed off-current of 100nA/μm, the researchers claim a record high on-current for III–V-FETs on-Si of 250μA/μm with 32nm gate length. With 20nm gates, the on-current was still respectable at ~200μA/μm.

Gallium nitride

Taiwan's National Chiao Tung University, Japan's Tokyo Institute of Technology and the USA's University of California Berkeley (UCB) have developed a gallium nitride (GaN) metal-insulator-semiconductor high-electron-mobility transistor (MIS-HEMT) with high threshold voltage for enhancement-mode operation [Session T5-4]. This was enabled by using a ferroelectric material in the gate stack. The team comments that this could be a promising candidate for next-generation GaN HEMT power devices after device and process optimization for long-term reliability.

High-power switching device applications need normally-off enhancement-mode operation transistors for fail-safe performance. An added benefit is lower power consumption. Unfortunately, without special processing, GaN devices tend to be normally-on (at 0V gate), i.e. 'depletion-mode', as it is termed. GaN is of interest for power applications due to its high critical field for breakdown, enabled by its wide bandgap. Further, the electron saturation velocity is high, allowing faster switching.

AlGaN/GaN was grown on silicon by MOCVD. ALD was used to grow ferroelectric hafnium zirconium dioxide

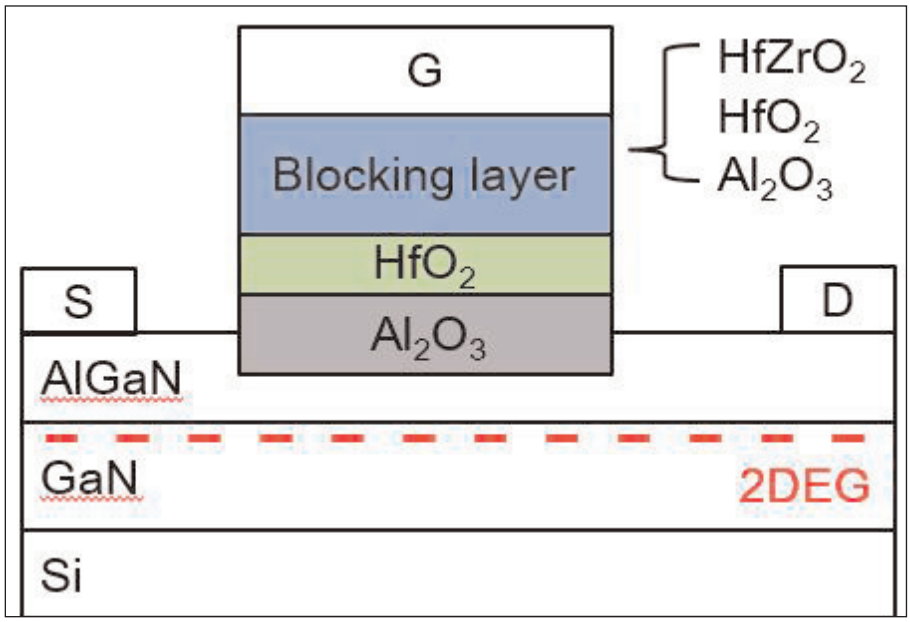


Figure 6. Schematic cross section of GaN MIS-HEMT.

($HfZrO_2$) blocking and ZrO_2 charge trap layers (Figure 6). The gate length was 2μm. The source–gate and drain–gate distances were 3μm and 15μm, respectively.

The threshold voltage was increased by applying 16V to the gate as an initialization step, causing polarization of the ferroelectric layer and charge trapping in the ZrO_2. The initialization step was less than 1ms.

This enabled a threshold voltage of +6V with a maximum drain current of 720mA/mm. The transconductance and on/off current ratio were 142mS/mm and $3x10^9$, respectively. Breakdown was at 1138V at 10μA/mm leakage. The threshold voltage shifted ~500mV at 0V drain bias after 10,000 seconds. The shift under 10V drain bias was ~300mV for the same time period.

Dynamic on-resistance under switching conditions was 1.6x the static on-resistance. The relatively modest current collapse is attributed to nitrogen passivation being applied before silicon nitride on the AlGaN barrier layer. An increase in the threshold voltage was seen in devices with a recessed gate — unfortunately the recessing also reduced the maximum drain current.

The $HfZrO_2$ blocking layer delivered both high threshold voltage and maximum drain current, compared with other enhancement-mode GaN devices. ■

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