

Trends toward low-cost, high-power, high-frequency devices on silicon and more

Mike Cooke reports on contributions to December's International Electron Devices Meeting in San Francisco.

The most recent International Electron Devices Meeting (IEDM 2019) in San Francisco, CA, USA in December continued the trend of researchers reporting the development of III-V compound semiconductor devices using a silicon (Si) substrate, aiming at significant reductions in production and deployment costs. The work is targeted at both power and radio frequency (RF) electronics. For the generation of wireless signals, one often wants both high power output and high frequency.

Up to now, gallium nitride (GaN)-channel devices on silicon have tended to be for the lower-frequency switching capabilities used in power conversion and management. This is because growing GaN and other III-nitride materials on silicon is difficult to achieve with high crystal quality. However, the work reported at the latest IEDM suggests that researchers are expanding the capabilities, looking to the exacting requirements needed for fifth-generation (5G)-and-beyond wireless communications technology.

Another interesting development for GaN was some inklings for ways to achieve decent p-channel transistors using III-nitride materials. Here, we look in greater detail at these developments and more.

Compound semiconductors on silicon

Power and high-frequency moves

IMEC and KU Leuven in Belgium reported co-integration of GaN power integrated circuits on 200mm-diameter silicon-on-insulator (SOI) substrates [session 4.4].

The use of SOI substrates avoids back-gating effects seen in silicon, providing the necessary electrical isolation of the devices.

Among the components deployed were 200V high-electron-mobility transistors (HEMTs), metal-insulator-metal (MIM) capacitors, Schottky barrier diodes (SBDs), and two-dimensional electron gas (2DEG) resistors (Figure 1). Resistor-transistor logic (RTL) was used to compensate for the lack of an effective p-channel field-effect transistor (FET) solution in GaN. A 48V-to-1V single-stage buck converter combined a GaN half-bridge and on-chip driver circuitry. The metal-organic chemical vapor deposition (MOCVD) epitaxial structure included a p-GaN top layer, providing a p-GaN gate, allowing enhancement-mode devices to be achieved.

IMEC/KU Leuven also joined with Taiwan's National Chiao Tung University, Vanderbilt University in the USA and Belgium's Vrije Universiteit Brussel (VUB) to present a complementary metal-oxide-semiconductor (CMOS)-compatible, gold-free process for aluminium gallium indium nitride (AlGaInN) HEMTs, metal-insulator-semiconductor HEMTs (MISHEMTs) and MOSFETs on 200mm silicon [session 17.2]. The devices were targeted 20GHz RF operation with low 0.15dB/mm transmission loss, along with low contact resistance of 0.14 Ω -mm. The vertical breakdown voltage (V_{BR}) was more than 300V. The field-effect mobility of the MISHEMTs exceeded 2000cm²/V-s.

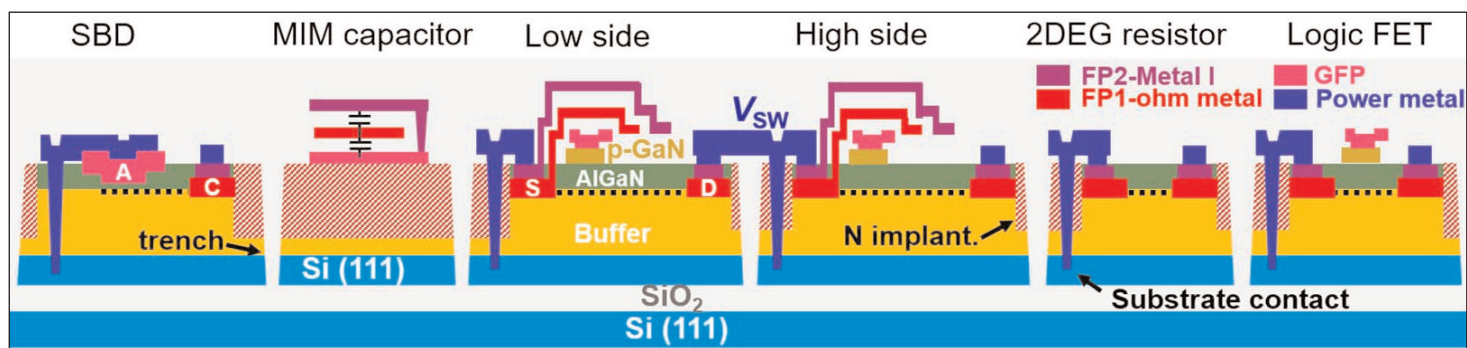


Figure 1. Schematic process cross-sections of GaN integrated circuit components on GaN-on-SOI substrate.

Such devices are sought for power amplification of radio signals for use in radar, satellite communication and wireless communication. The researchers comment: "Migrating to a 200mm silicon platform and manufacturing devices using standardized CMOS fab tools are critical steps toward the uptake of GaN devices for RF and mm-wave applications."

The ohmic contacts consisted of Si/Ti/Al/Ti/TiN recessed through the AlGaIn/AlN barrier layers. The gate metal was titanium nitride (TiN). The MISHEMTs and MOSFETs used 10nm and 25nm aluminium oxide (Al_2O_3) dielectric, respectively. Devices with AlInN barrier layers showed reduced on-resistance (R_{on}) and increased transconductance and on-current.

IMEC, KULeuven and VUB also reported the 'first' demonstration of III-V heterojunction bipolar transistors (HBTs) on 300mm-diameter silicon substrates [session 9.1]. The current gain was 112 and the breakdown voltage (BV_{CBO}) was 10V. The researchers see "potential for enabling a hybrid III-V/CMOS technology for 5G and mm-wave applications". The devices used a gallium arsenide/indium gallium phosphide (GaAs/InGaP) heterostructure.

The integration of III-V material used a selective nano-ridge aspect-ratio trapping process. The defects from GaAs heterointegration on silicon were trapped by high-aspect-ratio trenches, resulting in high-crystal-quality ridges. Further epitaxial layers were added using metal-organic vapor phase epitaxy.

The team comments: "HBTs fabricated on this stack show an electrical performance considerably better than GaAs(P) devices fabricated on a silicon substrate with SRB [strain-relaxed buffer] layers, without any need to grow thick (>1–10 μm) buffer layers."

Multi-channel boost

École polytechnique fédérale de Lausanne (EPFL) in Switzerland and Enkris Semiconductor Inc in China reported on multi-channel AlGaIn/GaN MOSHEMTs on silicon that showed reduced specific on-resistance $R_{\text{on,sp}}$ of 0.47 $\Omega\text{-cm}^2$ while maintaining a high V_{BR}

[session 4.1]. The performance was achieved using slanted tri-gates, rather than field plates, to enhance V_{BR} (Figure 2).

The team comments: "Firstly, the multi-channel devices broke the limit in R_{on} for lateral GaN power devices, greatly reducing the R_{on} from $\sim 7\Omega\text{-mm}$ in 600/650V single-channel devices to 2.8 $\Omega\text{-mm}$, while keeping a high V_{BR} of 1230V. In addition, the multi-channel devices yielded a record figure-of-merit of 3.2GW/ cm^2 that is substantially improved from single-channel devices."

The researchers used a stack of four 2DEG channels to reduce R_{on} . The team also developed an enhancement-mode device with a threshold voltage (V_{th}) of +0.9V for 1 $\mu\text{A}/\text{mm}$ drain current. The researchers comment: "These results significantly outperform conventional single-channel devices and demonstrate the enormous potential of multi-channel power devices."

The channel stack used $\text{Al}_{0.25}\text{Ga}_{0.75}$ barrier layers to achieve the 4x 2DEG structure. The bottom barrier was 10nm thick, while the top three were 20nm. The barriers were silicon-doped. The bottom layer was thinner and incorporated less doping with a view to improving electrostatic control, avoiding punch-through in the off state.

The structure achieved a sheet resistance of 80 Ω/square . The carrier sheet concentration and mobility were $5.6 \times 10^{13}/\text{cm}^2$ and 1407 $\text{cm}^2/\text{V-s}$, respectively. The researchers claim a record effective resistivity of 1.1m $\Omega\text{-mm}$ for the 140nm-thick structure.

The fin structures of the wrap-around tri-gate were continued into the source-drain region to allow easy low-resistance contact with all the 2DEG channels. The gate stack consisted of atomic layer deposition (ALD) silicon dioxide, and nickel/gold electrodes. The slanted gate fin widths were 50nm for 300nm, then increasing to 100nm for another 300nm. The gate region was 1.5 μm long in total, 700nm of which was covered in the gate stack. The enhancement-mode device used a fin as narrow as 20nm to increase the V_{th} . The leakage

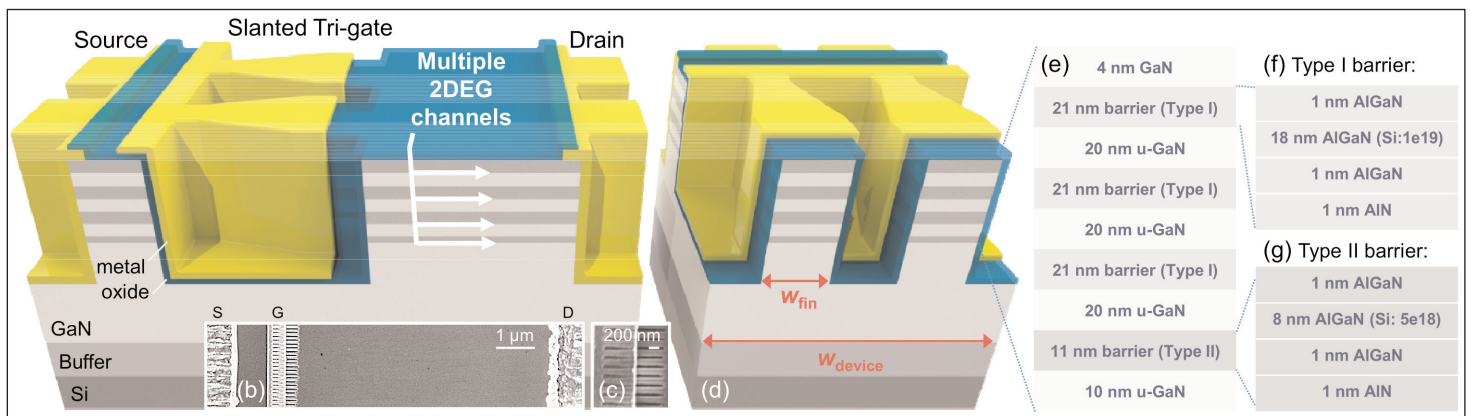


Figure 2. (a) Schematic of multi-channel slanted tri-gate MOSHEMTs. (b) Top-view, (c) zoomed scanning electron microscope images, and (d) cross-sectional schematic. (e)–(g) Schematics of the multi-channel structure with four parallel 2DEG channels.

of the normally-off transistor was 0.3nA/mm at 0V gate potential.

IBM Research Zurich and EPFL in Switzerland also reported on III-V heterojunction tunnel FETs integrated on 4-inch-diameter Si(100) substrates [session 37.1]. The devices feature InGaAs channels, heavily p-doped gallium arsenide antimonide (p⁺-GaAsSb) raised source contacts, and an n⁺-InGaAs drain. The team used a self-aligned CMOS-compatible process to create the transistors. The subthreshold swing was as low as 47mV/decade – so-called subthermionic behavior, since traditional transistors are usually limited by a temperature-dependent lower limit, 60mV/decade at 300K (a typical 'room temperature').

The researchers comment: "This is the first demonstration of sub-60mV/decade switching in heterostructure TFETs on Si(100), showing the strong promise of the technology for future advanced logic nodes aiming at low-power applications." A low swing allows lower supply voltage, reducing power consumption. The III-V materials were transferred to the silicon substrate by direct wafer bonding. The III-V drain and source materials were regrown using MOCVD.

5G and beyond

P-channel complement

Intel Corp in the USA reported the first heterogeneous integration of GaN NMOS and Si PMOS devices on 300mm-diameter high-resistivity silicon, targeting energy-efficient and compact power delivery, RF (5G and beyond) and system-on-chip applications [session 17.3]. The enhancement-mode NMOS transistors achieved 1.5mA/μm on-current, and off-currents as low as 100pA/μm. The f_T/f_{max} cut-off frequencies were 190/300GHz, respectively. Power amplification

circuits achieved power-added efficiencies of 56% at 28GHz and 70% at 5GHz.

The GaN transistors were created by MOCVD on Si(111). The Si PMOS integration used 3D layer transfer from another 300mm wafer (Figure 3).

Cornell University and Intel have meanwhile been working to fill the p-channel III-N transistor gap with a GaN/AlN heterostructure FET (HFET) achieving more than 100mA/mm on-current [session 4.5]. The researchers claim this as "the strongest on-current performance of any significantly modulating p-channel transistor in the III-nitrides." Combined with the more advanced n-channel III-N transistors, the work could enable the use of more efficient complementary circuit designs, as seen with mainstream CMOS silicon electronics. An on-current of 300mA/mm was reached in cryogenic measurements at 77K. The researchers point out that their p-channel devices are "within striking distance" of reported high-voltage extended-drain 65nm silicon CMOS pFETs that generally achieve around 200mA/mm.

The GaN/AlN structure generates a two-dimensional hole gas (2DHG) channel through the discontinuity in charge polarization of the GaN and AlN chemical bonds. The heterostructure was grown by plasma-enhanced chemical vapor deposition (PECVD) on 2-inch-diameter AlN/sapphire templates. The templates were produced by MOCVD.

The fabricated transistors had palladium/nickel source-drain contacts deposited on a p-InGaN layer. The recessed Schottky gate was a molybdenum-based metal stack on the exposed GaN layer. The researchers comment that at present there is no suitable dielectric for MOS structures on p-channel devices. The fabrication avoided the use of gold with a view to facilities

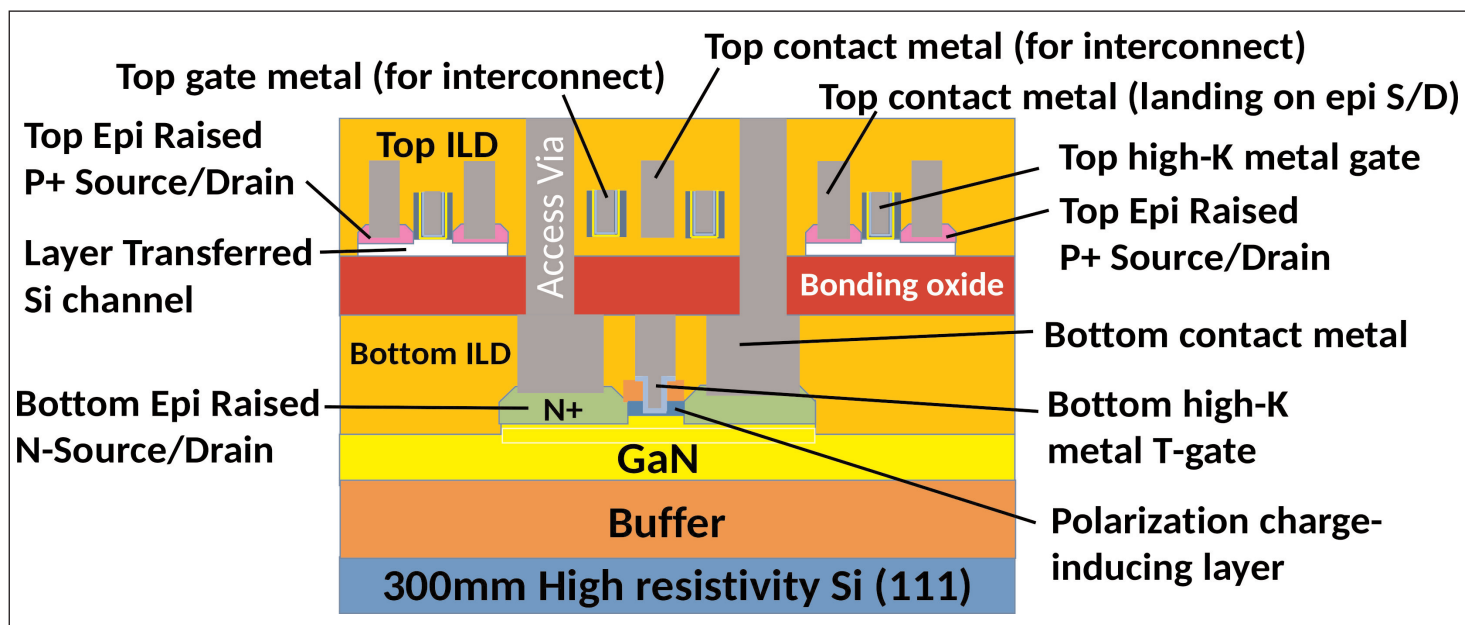


Figure 3. 3D heterogeneous integration of silicon PMOS transistors stacked on GaN NMOS transistor, enabled by 300mm GaN MOCVD epitaxy and 300mm 3D layer transfer.

where the metal is deprecated, such as in silicon wafer fabs.

Massachusetts Institute of Technology in the USA, Khalifa University in the United Arab Emirates (UAE), Enkris Semiconductor Inc in China and Intel in the USA reported on a self-aligned process for fabricating GaN pFETs [session 4.6]. The device used a GaN/Al_{0.2}Ga_{0.8}N/GaN structure grown on silicon by MOCVD. The R_{on} of 400Ω-mm is claimed to be a record low. The on-current was 5mA/mm, and the on/off current ratio was 6x10⁵.

The threshold of -1V implies a normally-off enhancement-mode operation in p-channel devices; the opposite is true in n-channel transistors, where positive thresholds are needed. The researchers demonstrated the potential for complementary nFET and pFET circuits by monolithically integrating such devices on the platform.

The researchers see the use of silicon substrates as promising low cost and integration with high-performance logic and analog functionality. The self-aligned process compensates for low hole mobility by allowing aggressive device scaling, in this case by creating a 100nm-gate-length pFET.

The MOCVD was carried out by Enkris on 6-inch-diameter silicon substrates. The structure sequence was a 3.8μm buffer, 150nm unintentionally doped (UID) GaN, 20nm AlGaIn, 20nm UID GaN, 50nm p-GaN, and 20nm p⁺-GaN.

The self-aligned process created nickel/gold/nickel source-drain stacks that presented a mask for mesa etch and gate recessing down through the p-GaN layers to the top 20nm UID GaN layer. The gate dielectric was ALD Al₂O₃. The gate electrode was nickel/gold. The nFET used the p-type layers as a p-gate (Figure 4).

Pushing over 100GHz

NTT Device Technology Labs and

Tokyo Institute of Technology in Japan presented a 300GHz wireless transceiver (TRx) aimed at 'beyond 5G' deployment (i.e. more than 10Gb/s data rate), based on indium phosphide HEMTs [session 9.2]. The channel material was high-mobility In_{0.8}Ga_{0.2}As on lattice-matched In_{0.53}Ga_{0.47}As.

The device supported data rates of more than 100Gb/s. The transmission distance was 2.2m, increasing to 9.8m for 120Gb/s data with the aid of a high-linearity power amplifier. According to the team, these rates are the highest achieved so far for electronic-device-based 300GHz TRx.

The frequency range above 275GHz is attractive since it is presently unallocated and offers much higher bandwidth. Further, these frequencies have attenuation rates of less than 10db/km. Since the wavelength of the radiation was comparable to the size of the device, special measures in the monolithic microwave integrated circuit (MMIC) design had to be implemented, such as using a backside DC line, to give a low-loss connection with the waveguide portion of the device.

NXP Semiconductors [session 25.2] reports the first "3.3V/5V RF-LDMOS with a cutoff frequency beyond 100GHz, designed and fabricated without any additional dedicated mask in an advanced sub-28nm node FDSOI process."

The researchers — based in Belgium, The Nether-

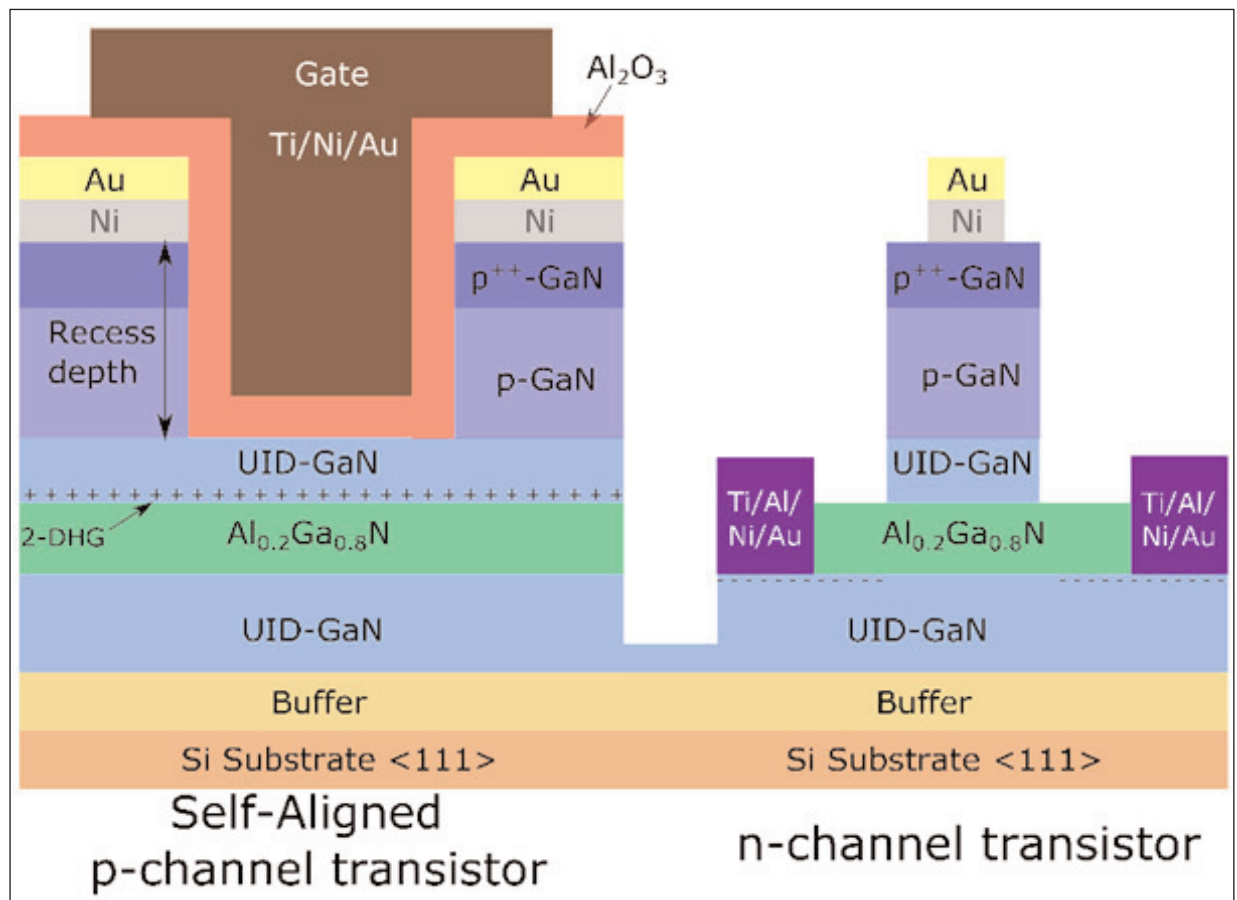


Figure 4. Monolithic integration of self-aligned p-FET and p-GaN gated n-FET.

lands, the USA and France — have also designed a series of passive devices for integration in the fully depleted SOI (FDSOI) process. They comment: “The RF performance of these high-voltage (HV)-capable devices is comparable to best-in-class devices in RF-HV-centric non-CMOS processes, e.g. SiGe and GaAs. This enables highly integrated cost-effective power amplifiers for both WiFi (5GHz) and 5G (28GHz) applications.”

It is hoped that the device platform could find application in watt-level RF power amplifiers for WiFi, 5G, and beyond.

ETH-Zürich in Switzerland claims the first demonstration of “high-performance HEMTs combining InAs channel insets with InP sub-channels” [session 9.3]. The technique reduced the minimum noise figure to 0.65dB at 40GHz, compared with 1.15dB without an InP sub-channel. The inset in the 0.65dB case was 3nm and in the 1.15dB device it was 5nm. A 5nm inset with sub-channel achieved a 0.93dB minimum noise. The structure was designed to reduce noise from impact ionization. Applications of such devices presently center on radio-astronomy and deep-space communication. The f_T/f_{max} cut-off frequencies were 410GHz/660GHz, respectively.

Gallium oxide and silicon carbide

Substrate

Fraunhofer Institute for Applied Solid State Physics IAF in Germany claims the highest ever power-added efficiency for L-band (1–2GHz) performance of 77.3% at 1.0GHz [session 17.4].

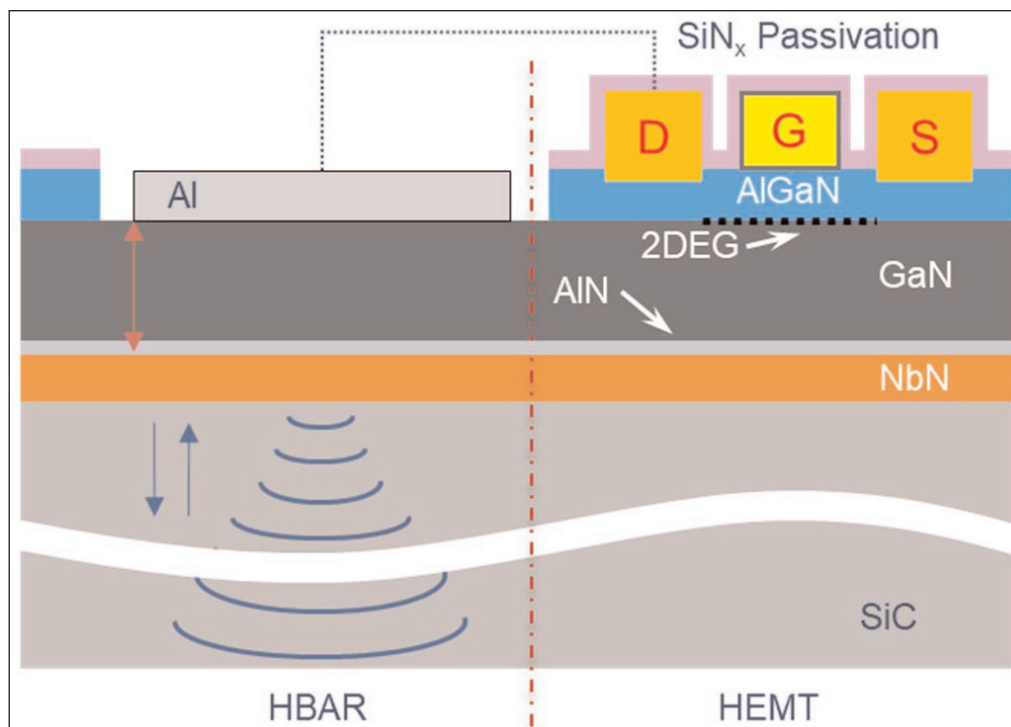


Figure 5. Cross-sectional schematic of HBAR+HEMT integrated on AlGaIn/GaN/NbN heterostructure.

The 0.5 μ m-gate transistor used an AlGaIn/GaN structure on a 4-inch-diameter silicon carbide (SiC) substrate and was optimized for 100V load-pull operation. The maximum power density was more than 17W/mm with the drain biased at 100V. This increased to 20W/mm at 125V. The enhanced performance and power density was enabled by increasing the supply voltage to 100V, compared with the 28–50V used for mobile communications or civil and military radar.

To improve the high-voltage performance, the researchers optimized the extension of the source-terminated field plate (STFP) towards the drain contact, balancing the need for high V_{BR} against increased parasitic source-drain capacitance. The measured breakdown was more than 500V. The transistors also featured gate-terminated field plates.

The MOCVD epitaxial structure used a semi-insulating iron-doped GaN buffer on an AlN nucleation layer. The AlGaIn barrier was capped with GaN.

The US Naval Research Laboratory reported integration of GaN HEMTs with a high overtone bulk acoustic resonator (HBAR) on SiC substrate [session 17.5]. The device achieved what is described as high values of quality factor (Q) and Q x frequency product at 295K of more than 10^4 and 10^{14} Hz, respectively

The combination of HBAR and HEMT is expected to lead to “building blocks for comb filters, circulators, and sparse spectrum front-ends”. The superconducting nature of the niobium nitride (NbN) also suggests to the team that the structure has “enormous potential as an integrated quantum platform for computation, communications, sensing, and metrology”. The Q-factor was more than 10^6 at 20K.

The molecular-beam epitaxy (MBE) structure consisted of a transition-metal nitride buried NbN electrode, and GaN buffer and AlGaIn barrier layers (Figure 5). The acoustic waves were generated by piezoelectric stressing between an Al electrode and the buried NbN.

The combined structure demonstrated an on/off gain of 34dB (more than 10^3) in forward transmission (S_{21}) and a 16dB (factor of 40) directional contrast at 3GHz.

The researchers comment: “The amplified HBAR+HEMT pair can be used in a ladder configuration in order to generate exquisitely sharp RF comb filters, with zero loss, or net terminal gain. This configuration can be used to realize on-chip integrated oscillators

with low phase noise, or magnet-free frequency-selective integrated circulators operating beyond the X-band.”

Vertical power

Researchers from the USA and Japan claimed record-high performance for normally-off single- and multi-fin gallium oxide ($\beta\text{-Ga}_2\text{O}_3$) vertical power transistors [session 12.4]. The team from Cornell and Hosei universities used an anneal process at 350°C for 1 minute in nitrogen after the metal electrode deposition to increase channel mobility to $\sim 130\text{cm}^2/\text{V}\cdot\text{s}$. With the fin width at $0.15\mu\text{m}$, the V_{th} was more than +1.5V, giving true normally-off performance.

Multi-fin devices (Figure 6) managed to push breakdown voltages up to 2.66kV. The $R_{\text{on,sp}}$ was $25.2\text{m}\Omega\cdot\text{cm}^2$, corresponding to a Baliga figure of merit of $280\text{MW}/\text{cm}^2$. The figure of merit expresses the trade-off between V_{BR} and $R_{\text{on,sp}}$ as $V_{\text{BR}}^2/R_{\text{on,sp}}$. The researchers claim that the $280\text{MW}/\text{cm}^2$ value is the highest reported for all Ga_2O_3 transistors (Figure 7).

The team also found that fins with approximately (100) sidewalls showed reduced interface trapping effects and higher current compared with other orientations relative to the crystal structure.

The Ga_2O_3 was deposited using halide vapor phase epitaxy (HVPE). The $10\mu\text{m}$ drift layer had a net n-type doping concentration of $2\times 10^{15}/\text{cm}^3$, according to capacitance-voltage studies.

Researchers from China,

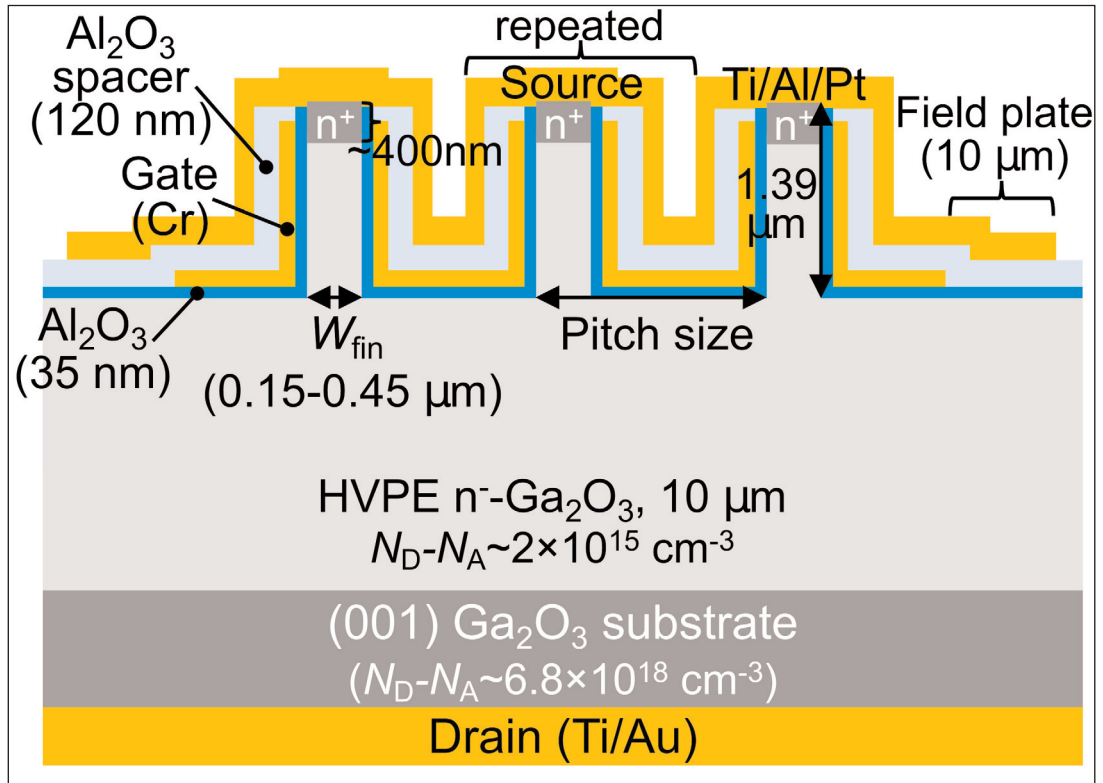


Figure 6. Schematic cross-section of Ga_2O_3 vertical fin transistors with multiple fins and source-connected field plate.

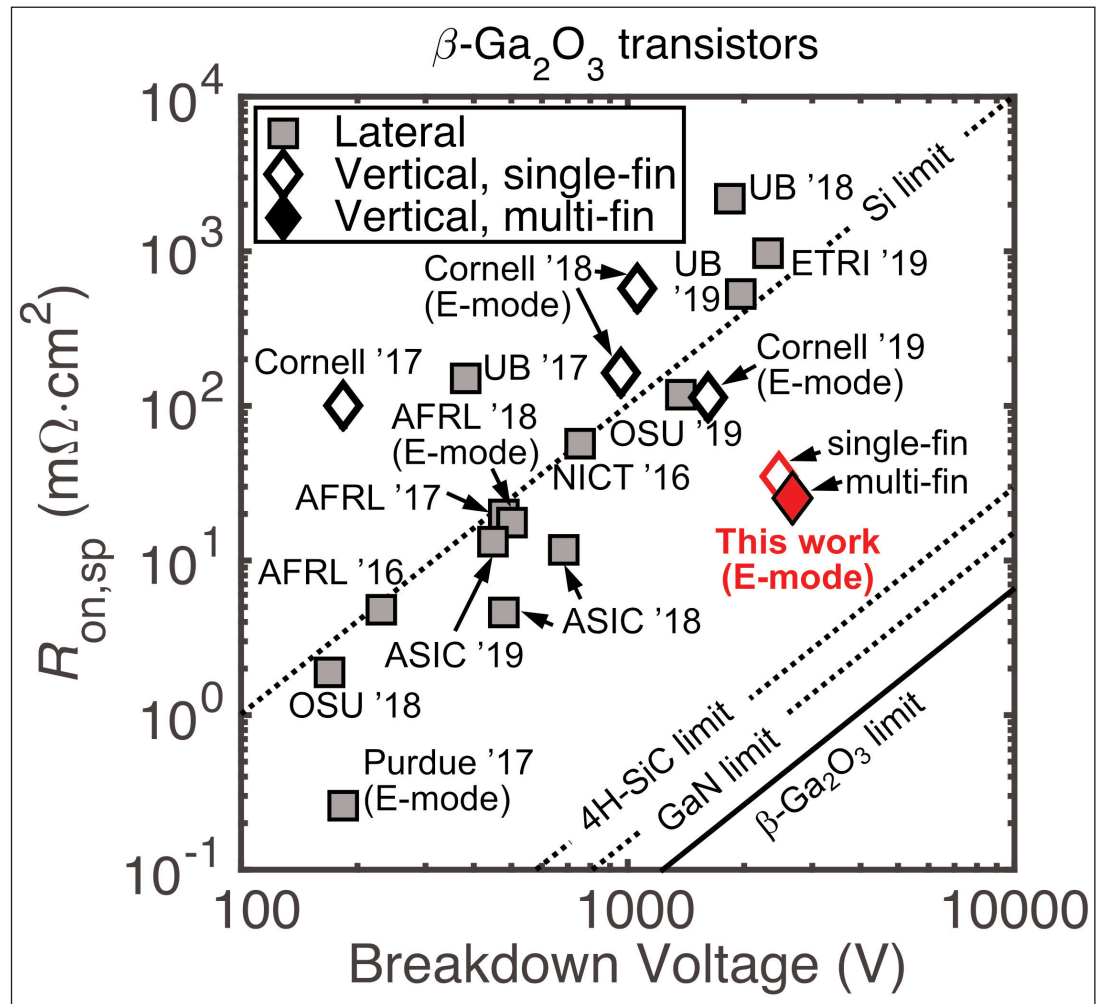


Figure 7. Benchmark plot of Ga_2O_3 transistors.

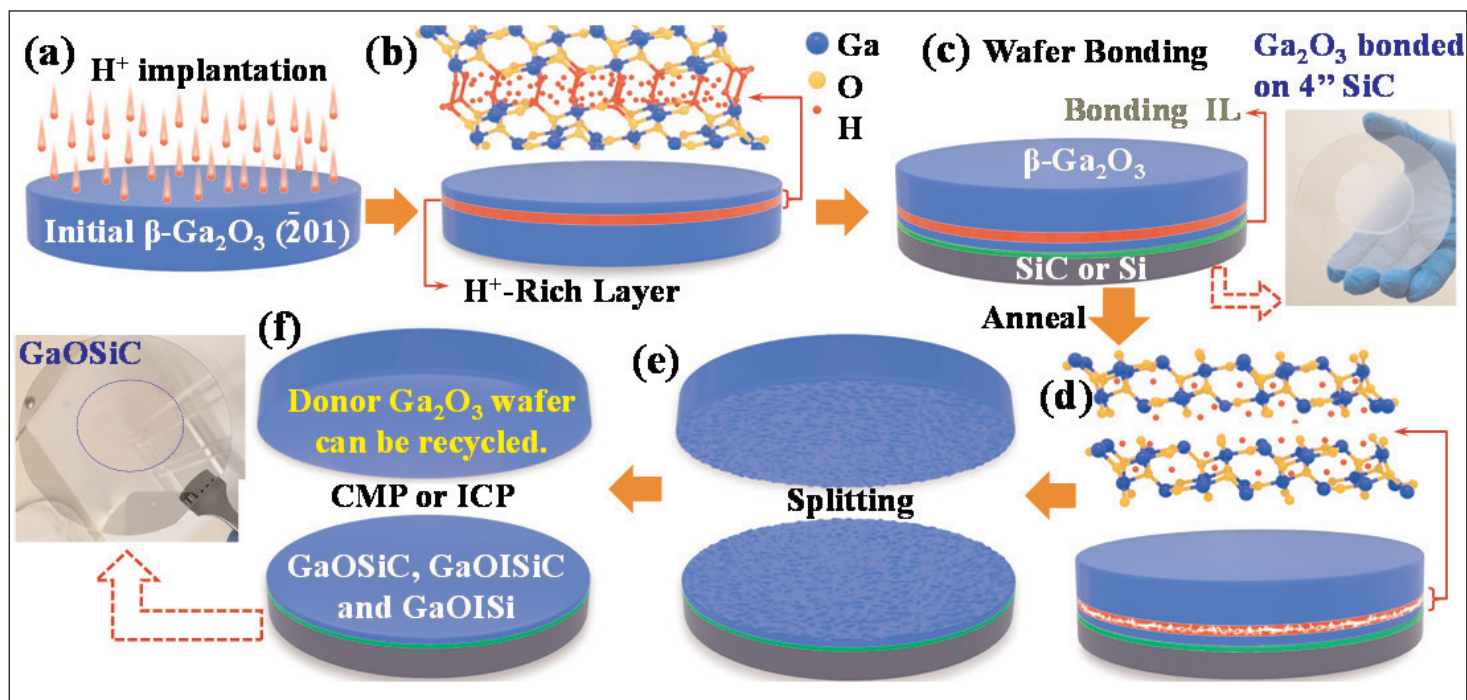


Figure 8. Process flow for transferring $\beta\text{-Ga}_2\text{O}_3$ thin film onto SiC (or Si) by ion-cutting. (a)-(b) Implanting H⁺ into bulk $\beta\text{-Ga}_2\text{O}_3$ (c) Wafer bonding onto SiC (or Si), using amorphous or Al_2O_3 interlayers. (d) Forming plate-like defects by annealing. (e) Splitting. (f) Surface smoothing. Fabricated Ga_2O_3 on SiC wafer shown.

Japan and the USA say that they have demonstrated “for the first time” the transfer of 2-inch-diameter thin Ga_2O_3 layers to Si and SiC substrates using ion-cutting methods [session 12.5]. The team from Shanghai Institute of Microsystem and Information Technology and Xidian University in China, Meisei University in Japan, and Virginia Polytechnic Institute and State University in the USA also produced high performance enhancement-mode/depletion-mode normally-off/-on metal-oxide-semiconductor FETs on the material. They were also able to produce material with an insulating aluminium oxide interlayer.

A device operated at 500K maintained a V_{BR} above 600V. The researchers see the use of a thin Ga_2O_3 film as a means to overcome one of the drawbacks of the material — its low thermal conductivity compared with Si and SiC, enabling better thermal stability of devices.

The technique used for the transfer is related to the commercial SmartCut process trademarked to SOITEC (Figure 8).

The less than 400nm films demonstrated 0.5nm root mean square roughness and 130arcsec x-ray diffraction rocking curve full-width at half maximum (FWHM). Wafer-level Ga_2O_3 thickness non-uniformity was $\pm 1.8\%$. The smooth surface was achieved after wafer bonding with inductively coupled plasma etch (2.0nm roughness) or chemical mechanical planarization (0.5nm roughness.)

Thyristor-IGBT combo

Japan’s National Institute of Advanced Industrial Science and Technology (AIST) claims the first fabrication of a 17kV SiC MOS thyristor combined with insulated-

Mitsubishi Electric Corp and the University of Tokyo in Japan have been the first to use oxygen ion-implant doping in the channel of SiC MOSFETs

gate bipolar transistor (IGBT) [session 20.2]. The on-voltage was 5V and the differential on-resistance was $15\text{m}\Omega\text{-cm}^2$ at 100A/cm^2 current density. An IGBT produced on the same process achieved 5.03V and $17\Omega\text{W-cm}^2$, respectively.

Raising the temperature to 423K did not degrade the MOS thyristor performance. The switching operation and speed were comparable to those of IGBTs in terms of turn-on and -off performance.

Mitsubishi Electric Corp and the University of Tokyo in Japan have been the first to use oxygen ion-implant doping in the channel of SiC MOSFETs [session 20.4]. The effect was to reduce channel resistance and increase the V_{th} . The oxygen doping creates deep-level donor states. Conventional SiC MOSFET doping involves sulfur. The team comments: “By applying this novel technique to vertical 4H-SiC MOSFETs, 32% reduction of specific on resistance (R_{on}) at a high V_{th} of 4.5V was achieved.”

The device was also found to have improved negative bias temperature instability (NBTI) performance in terms of V_{th} . The use of ion-implant doping gave a higher concentration near the MOS interface compared with thermal oxidation doping processes. The gate oxide was produced by thermal oxidation, followed by nitridation using a diluted NO atmosphere. ■

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