

Laser annealing enables gate-first fabrication of III-nitride transistors

A localized technique also results in 27% higher drain current than gate-last global rapid thermal processing.

South China University of Technology has used focused laser light to perform selective, micron-scale localized annealing of source and drain electrodes to enable gate-first fabrication of aluminium gallium nitride (AlGaN) high-electron-mobility transistors (HEMTs) [Zhikun Liu et al, IEEE Electron Device Letters, vol 39, issue 12 (December 2018) p1896].

Gate-first fabrication is standard in self-aligned silicon CMOS transistor fabrication. Adding gate-first GaN HEMT fabrication to the process palette could lead to novel integration options with Si CMOS such as creating new classes of digitally assisted RF mixed-signal and power conditioning circuits.

Typically, it would be preferred that the CMOS elements be processed before the AlGaN HEMTs. Unfortunately, thermal budgets of CMOS processing generally have an upper limit of 450°C to ensure that electrical

performance is maintained. HEMT fabrication normally uses gate-last process flows because achieving ohmic contacts for source and drain electrodes needs very high temperatures of more than 800°C that would damage gate structures. These temperatures also clearly bust the thermal budget for silicon CMOS.

The HEMT structure consisted of a 20nm Al_{0.25}Ga_{0.75}N barrier layer on a 150nm GaN channel/buffer. The two-dimensional electron gas (2DEG) channel was formed near the GaN/AlGaN interface with 1.0x10¹³/cm² carrier density, 1.5x10³cm²/V-s mobility, and 450Ω/square sheet resistance.

The gate-first fabrication process flow began with plasma-enhanced chemical vapor deposition (PECVD) of 20nm of silicon dioxide. Electron-beam evaporation of nickel/gold gate metals was followed by patterning via lift-off lithography into 5µm-long, 600µm-wide gate

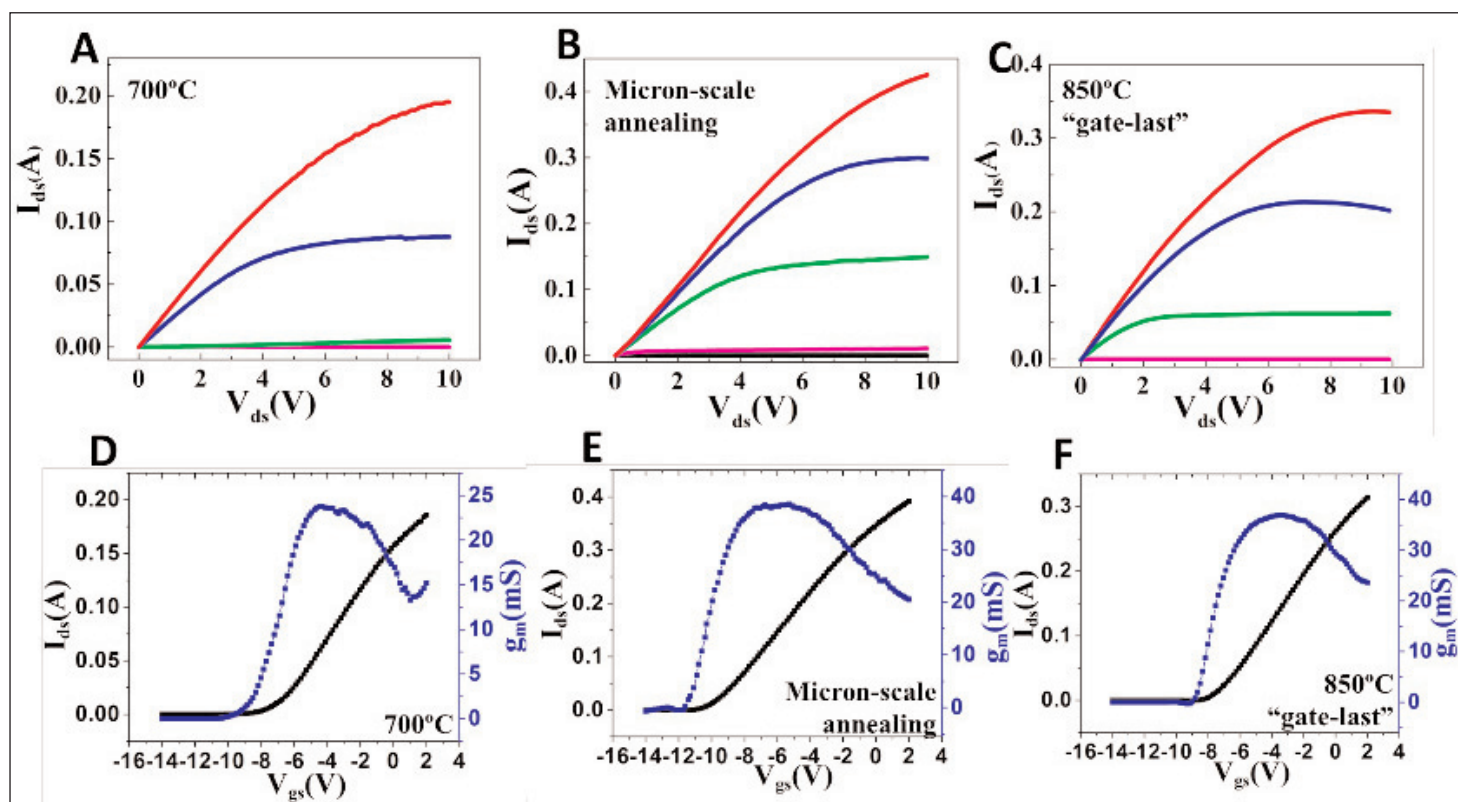


Figure 1. Output (A, B and C) and transfer characteristics (D, E and F) of devices processed by 700°C RTA, micron-scale annealing and gate-last approach, respectively.

structures. Patterned buffered oxide etching was used to remove the silicon dioxide insulation from the source/drain contact regions. Further electron-beam evaporation resulted in titanium/aluminium/nickel/gold source/drain electrodes. The source-gate and drain-gate spacings were 5 μm and 10 μm , respectively.

The annealing of the source/drain electrodes was achieved using 532nm continuous-wave laser light focused to a 3 μm spot by a microscope objective lens. The aim was to thermally activate the out-diffusion of nitrogen from the AlGaN. The process was carried out in a home-made vacuum chamber at 5 $\times 10^{-3}$ Pa pressure. Vacuum was critical for avoiding oxidation during annealing.

The laser spot scanned twice over the electrodes at 10 $\mu\text{m/s}$ speed. The laser power was between 0.84W and 0.96W for low-resistance contacts — the optimum was around 0.9W. Simulations suggested that the temperature at the center of the laser spot would be 850 $^{\circ}\text{C}$ after 0.5s, while 6.5 μm away the temperature would fall to 335 $^{\circ}\text{C}$.

Contact resistance as low as 0.3 $\Omega\text{-mm}$ was achieved (2.2 $\times 10^{-6}\Omega\text{-cm}^2$ specific contact resistance). The researchers attribute the low contact resistance to the formation of a thicker $\sim 35\text{nm}$ titanium nitride layer compared with the $\sim 10\text{nm}$ of more conventional rapid thermal annealing (RTA). The thicker titanium nitride layer of the laser anneal is correlated with the formation of nitrogen vacancies in the underlying AlGaN, leading to the formation of an ohmic contact. Also, the fast temperature rise of $\sim 2\text{s}$ allows nitrogen to escape through the titanium before titanium nitride crystallization at the interface.

Comparison gate-last devices were created with source/drain electrodes annealed rapidly at 850 $^{\circ}\text{C}$ for 1 minute before reactive ion etching of the mesa and silicon dioxide deposition and gate formation. The contact resistance for this method was 0.8 $\Omega\text{-mm}$ (7.2 $\Omega\text{-mm}$ for 700 $^{\circ}\text{C}$ annealing). Another effect of 850 $^{\circ}\text{C}$ RTA was to increase the sheet resistance of the 2DEG to 600 Ω/square , according to transmission-line method measurements. Further comparison devices were fabricated gate-first with lower-temperature RTA at

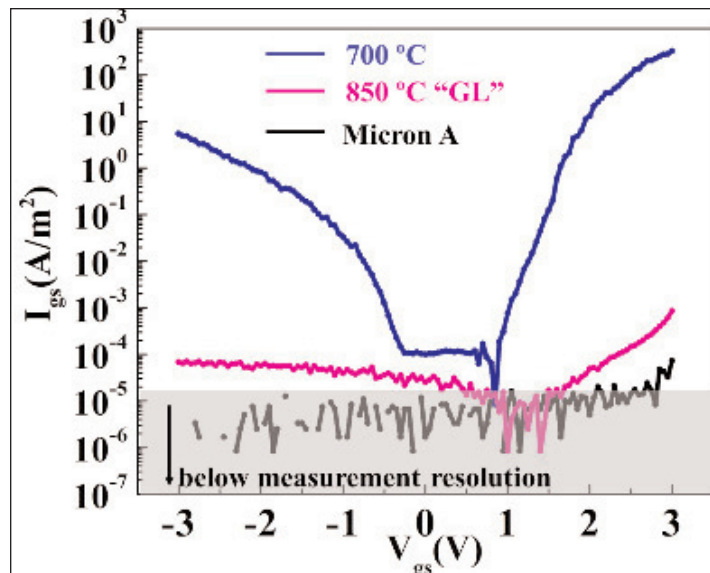


Figure 2. Gate current density-voltage (I_{gs} - V_{gs}) characteristics of GaN MOSFETs processed by RTA at 700 $^{\circ}\text{C}$, micron-scale annealing and gate-last approaches.

700 $^{\circ}\text{C}$ and 800 $^{\circ}\text{C}$. The 800 $^{\circ}\text{C}$ anneal destroyed the gate, while at 700 $^{\circ}\text{C}$ the gate became defective, according to optical inspection.

The electrical performance of the gate-first micron-scale laser-annealed HEMTs showed higher drain current and transconductance compared with 700 $^{\circ}\text{C}$ RTA gate-first and 850 $^{\circ}\text{C}$ gate-last devices (Figure 1). With the gate at 2V, the maximum drain current for gate-first micron-scale annealing was 0.42A — 110% higher than for the 700 $^{\circ}$ gate-first HEMT and 27% than the 850 $^{\circ}\text{C}$ gate-last device.

The researchers point out that the profile of the transconductance laser-annealed device was flatter, suggesting better linearity and larger dynamic range in applications.

Micron-scale annealing also limited gate leakage to less than 7 $\times 10^{-5}\text{A/m}^2$ — comparable to the gate-last device and a factor of 10^6 lower than the gate-first 700 $^{\circ}\text{C}$ HEMT (Figure 2). ■

<https://doi.org/10.1109/LED.2018.2877717>

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