Getting the best cost and performance out of GaN-on-silicon devices

Mike Cooke looks at recent research to realize better-performing and more complex transistors and diodes.

Gallium nitride (GaN) transistors and diodes are being developed for power electronics applications with a view to replacing the present pure silicon components. The wide bandgap of GaN offers opportunities to increase carrier saturation velocities, mobility and density, along with higher critical electric field for higher breakdown voltages. However, these opportunities will only be realized if GaN-based devices can be produced at sufficiently low cost to compete with silicon alternatives.

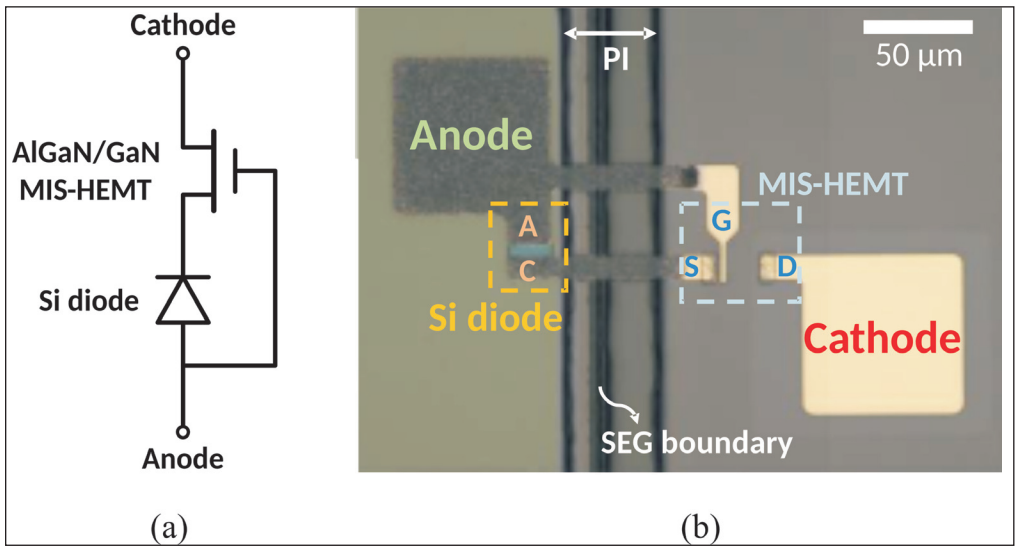


Figure 1. (a) Circuit schematic and (b) top-view image of cascoded diode.

An obvious route to less expensive devices is to use III-nitride materials grown on large-diameter silicon substrates, which costs a fraction of the amount needed to buy more conventional — and smaller-diameter — substrates such as sapphire, silicon carbide (SiC) or free-standing GaN. Another cost-cutting technique is to increase device density, improving wafer utilization efficiency.

Here, we look at some recent research to realize better-performing and more complex GaN power electronics on silicon substrates.

Cascode diode

Hong Kong University of Science and Technology (HKUST) has developed a high-voltage monolithic cascode diode combination (Figure 1) of silicon (Si) pn diode and normally-on aluminium gallium nitride (AlGaN) barrier metal-insulator-semiconductor high-electron-mobility transistor (MIS-HEMT) [Jie Ren et al, IEEE Electron Device Letters, vol38, p501, 2017].

"Compared with conventional AlGaN/GaN [Schottky barrier diodes (SBDs)], the cascoded diode can provide much lower reverse leakage current due to the superior voltage-blocking capability of the MIS-HEMT and the low leakage of the Si diode," the researchers comment.

The researchers also see the monolithic integration work as leading to smaller effects from parasitic inductance, resistance or capacitance compared with systems assembled from a number of discrete parts. "Large parasitics will cause circuit ringing during fast switching, resulting in system instability," they add. Further potential advantages include reduced system size and production cost.

The devices were fabricated on 4-inch (111) Si substrates (Figure 2). A 300nm layer of silicon dioxide was formed, which was etched to form a mask for the recessed window. Further etching created a 4mm-deep region for selective epitaxial growth (SEG). More silicon dioxide was deposited as a sacrificial layer that was then removed to smooth the bottom silicon surface in the recessed windows.

A new 1.5mm SiO_2 SEG mask was applied before metal-organic chemical vapor deposition (MOCVD) of a 280nm AlN nucleation layer, a 1.1µm step-graded AlGaN buffer, a 2.7µm GaN buffer, a 100nm GaN channel, a 1nm AlN spacer, 20nm $Al_{0.3}Ga_{0.7}N$ barriers, and a 8nm in-situ silicon nitride cap.

Polycrystalline GaN on the SiO_2 mask was removed

with dry etching that stopped at the SiO_2. Removing the SEG mask then resulted in a near-planar surface, which enabled fine-pattern lithography.

The p- and n-type regions of the silicon pn diode were formed by implantation of boron/boron difluoride (BF_2) and phosphorus, respectively. Plasma-enhanced chemical vapor deposition (PECVD) was used to create a 350nm SiO_2 passivation layer for the diode.

The AlGaN/GaN HEMT was fabricated by argon implantation defining the active region, selective etch of source-drain windows in the silicon nitride cap, titanium/aluminium/nickel/gold source-drain metal deposition, 830°C annealing to activate the Si diode doping and alloy the HEMT source-drain metal stacks, atomic layer deposition (ALD) of aluminium oxide as part of the gate insulator with the silicon nitride cap, and nickel/gold evaporation of the gate electrode.

The devices were connected using sputtered aluminium. A 2.5μm imide layer at the periphery of the SEG window improved the step coverage of the aluminium interconnect. The sputtered aluminium was also used to create the silicon pn diode contacts.

The silicon pn diode had a 50μm^2 active region with a drift region 2.5μm long and 20μm wide. The active MIS-HEMT area was 190μm^2 with 2μm-long 10μm-wide gate. The gate-source and gate-drain distances were 2μm and 15μm, respectively.

The interconnect distance of 70μm reduces the parasitic inductance to around 0.03nH, compared with the ~2nH typical for conventional ~2mm wirebonding.

Individual characterization of the silicon diode gave a forward voltage of 0.8V at 500A/cm^2 current density. Breakdown occurred at 22V. Meanwhile, the MIS-HEMT had an on/off current ratio of 10^8 and 613mA/mm drive current at 2V gate potential and 10V drain bias. The threshold voltage was –5.2V. Breakdown with 1mA/mm current density was 550V.

The cascode circuit had a turn-on voltage of 0.6V for a current density of 1A/cm^2, normalized by the sum of the active areas (240μm^2 = 50μm^2 + 190μm^2) of the component parts. At 500A/cm^2, the specific on-resistance was 5.4mΩ-cm^2 (differential, 2.8mΩ-cm^2).

A conventional AlGaN/GaN Schottky barrier diode on the same wafer had a 0.7V turn-on and 3.7mΩ-cm^2 specific on-resistance (1.8mΩ-cm^2, differential). The higher on-resistance of the cascode diode is blamed on "series resistance and the additional device area needed for the Si diode".

By contrast, the reverse bias leakage was two orders of magnitude lower for the cascode diode than for the SBD. In fact, the large reverse leakage of the SBD makes it impractical for applications, according to the researchers. In numbers, the cascode diode reverse leakage was 5.6x10^{-5}mA/mm (1.9x10^{-4}mA/cm^2) at 300V. The 300V reverse bias is a typical bus voltage for applications using 500–600V-class diodes, according to the team.

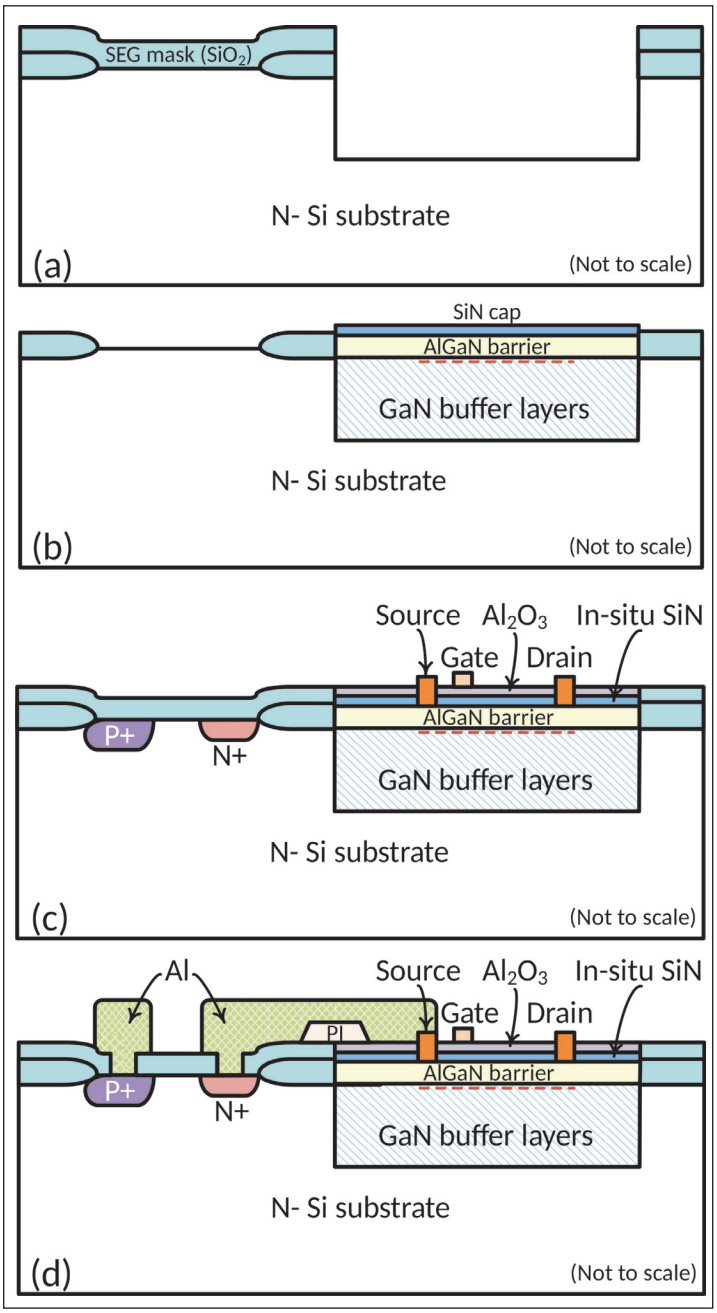


Figure 2. Schematic cross sections: (a) after recessed window formation, (b) after AlGaN/GaN epitaxial structure growth, (c) after Si and GaN fabrication, (d) after metal-line interconnection deposition.

The cascode diode reverse leakage performance was "smaller than most of the state-of-the-art AlGaN/GaN SBDs," the researchers say. They attribute the small leakage to "the superior voltage blocking capability of the MIS-HEMT and the low leakage current of the Si diode".

The cascode diode on/off current ratio was 3x10^6 with 1A/cm^2 breakdown of 557V, which the researchers claim is 62V greater than that of the conventional AlGaN/GaN Schottky barrier diode.

Another area where the cascode diode improves on the AlGaN/GaN SBD is in having a low ideality factor of 1.4, compared with 2.7, indicating a sharper turn-on behavior.

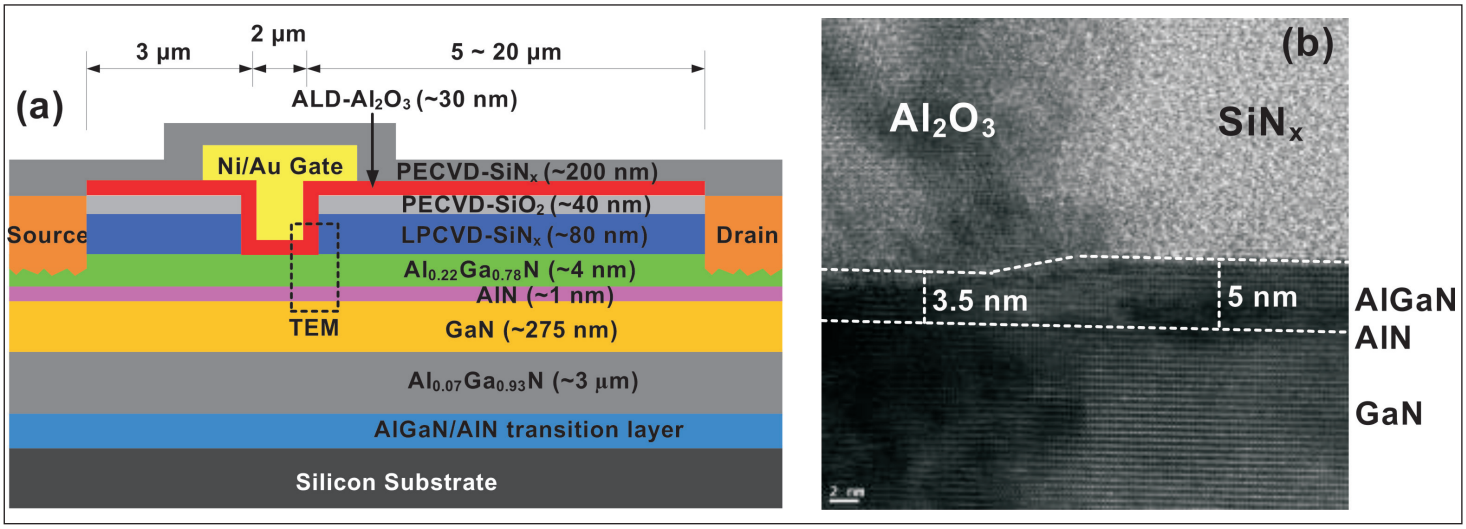


Figure 3. (a) Schematic device structure of normally-off Al_2O_3/AlGaN/GaN MIS-HEMTs fabricated on UTB AlGaN/GaN heterostructures. (b) Transmission electron microscope cross-sectional view of device's gate corner.

Varying the temperature between 25°C and 200°C, the reverse leakage of the cascode diode increased by two orders of magnitude, but this change was smaller than that of the AlGaN/GaN SBDs.

Ultra-thin-barrier

Researchers in China and Hong Kong have fabricated ultra-thin barrier (UTB) aluminium gallium nitride (AlGaN) on gallium nitride normally-off MIS-HEMTs with silicon nitride (SiNx) passivation [Sen Huang et al, IEEE Electron Device Letters, vol37, p1617, 2016]. The passivation reduced sheet resistance in the conducting two-dimensional electron gas (2DEG) near the AlGaN/GaN interface by almost an order of magnitude.

The team from the Institute of Microelectronics of the Chinese Academy of Sciences (CAS), the Suzhou Institute of Nano-Tech and Nano-Bionics in China, and the Hong Kong University of Science and Technology (HKUST) sees potential application in next-generation normally-off power-switching devices. Rather than using recess etch of thick AlGaN layers to achieve normally-off behavior, the researchers used a combination of ultra-thin barrier layers and passivation in the access regions (Figure 3).

The epitaxial material was grown by MOCVD on 4-inch silicon substrate. The ultra-thin AlGaN barrier on an AlN interface enhancement layer resulted in a 2DEG with $2.7x10^{12}/cm^2$ carrier density and 2570Ω/square sheet resistance.

Passivation with low-pressure chemical vapor deposition (LPCVD) of 80nm silicon nitride increased the sheet carrier density to $9.5x10^{12}/cm^2$. At the same time, the sheet resistance was reduced to 334Ω/square. The 2DEG mobility was increased to $1980cm^2/V\text{-}s$ from the $869cm^2/V\text{-}s$ value without passivation. The high mobility is taken as indicating insignificant interface roughness scattering.

The researchers calculated a positive surface charge of $4.56x10^{12}/cm^2$ at the silicon nitride/III-nitride interface from capacitance-voltage measurements. The team further estimates a reduction in the AlGaN surface potential from 1.35eV to 0.49eV. They comment: "The reduction of surface potential of AlGaN barrier by LPCVD-SiN_x contributes to an effectively enhanced 2DEG density in UTB AlGaN/GaN heterostructures."

To fabricate devices, the source-drain regions of the silicon nitride were etched using an inductively coupled plasma (ICP) mix of fluorform (CHF_3) and sulfur hexafluoride (SF_6). The exposed AlGaN was treated with hydrochloric acid. Titanium/aluminium/nickel gold ohmic contacts were deposited and annealed at 830ºC in nitrogen.

The gate region was also defined by fluorine-based ICP etch. Aluminium oxide (Al_2O_3) gate dielectric was applied using atomic layer deposition. Remote plasma pre-treatment of the Al_2O_3 deposition surface was used to suppress deep states at the Al_2O_3/AlGaN interface. The gate electrode was nickel/gold.

The maximum drain current of a MIS-HEMT with 2μm gate length was 661mA/mm at 12V gate potential. The specific on-resistance was 9.0Ω-mm. The gate–drain distance was 10μm. With 1V drain bias, the gate threshold (V_{TH}) for 1μA/mm current was +0.27V. Across a sample of 30 devices, the threshold standard deviation was 0.15V.

The researchers comment: "Owing to the as-grown ultra-thin AlGaN barrier, intentional recess etching of the AlGaN barrier is eliminated, contributing to improved V_{TH} controllability and uniformity."

The vertical breakdown voltage was 695V. Three-terminal breakdown occurred at 1089V, according to a leakage criterion of 1μA/mm with substrate floating. The breakdown path was source to drain. The three-terminal breakdown voltage reduced to 617V with a 5μm gate-to-drain distance.

Operation with 200ns pulses at 10µs period increased dynamic on-resistance by 10% (Figure 4), indicating some current collapse. The researchers suggest that the increased resistance could be due to oxidation during transfer between AlGaN barrier surface cleaning and growth of the silicon nitride passivation. Alternatively, border/bulk traps could be present in the passivation.

Devices with 20mm gate width achieved normally-off operation with 0.75Ω on-resistance and maximum drain current of 6.5A.

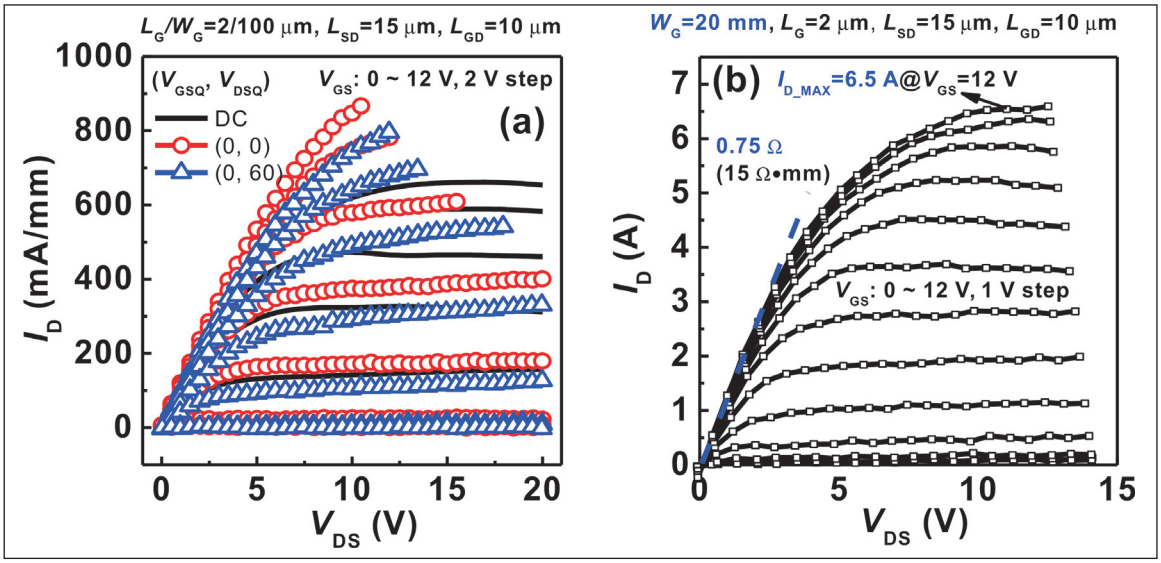


Figure 4. (a) Pulsed drain current (I_D) versus drain bias (V_{DS}) characteristics of fabricated normally-off Al_2O_3/AlGaN/GaN MIS-HEMTs from various quiescent gate, drain bias points (V_{GSQ},V_{DSQ}). (b) Characteristics of fabricated 20mm-gate-width devices.

Multi-level metalization

Researchers based in USA and Korea have used multi-level metalization to improve the performance and density of aluminium gallium nitride/gallium nitride (AlGaN/GaN) heterostructure field-effect transistors (HFETs) on silicon [Seung Kyu Oh et al, Appl. Phys. Express, vol10, p016502, 2017].

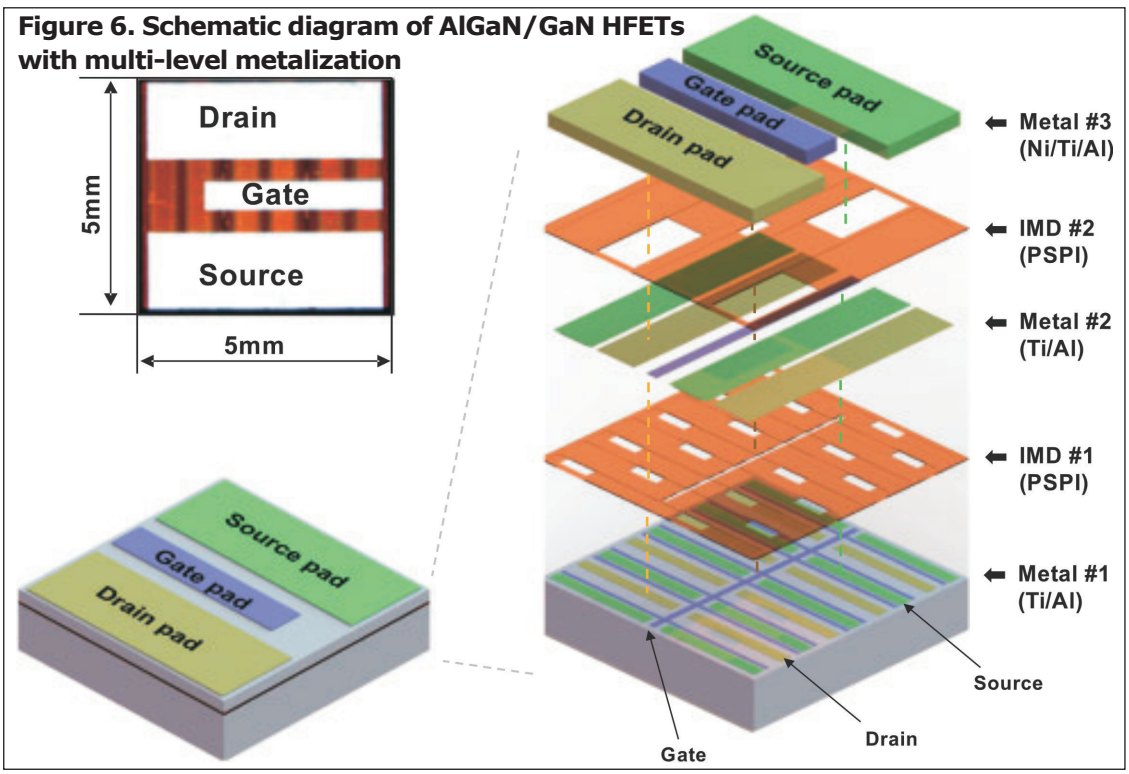
The devices achieved higher drain currents and lower fall off in current at high drain bias, compared with conventional single-metal-layer HFETs of the same device area. The team from the University of Houston in the USA and Sunchon National University, Chonbuk National University and LG Electronics in South Korea comments: "Multi-level metalization schemes, which are well developed in the Si-based semiconductor industry, are an effective way to increase the number of dies per wafer."

The III-nitride hetero-structure (Figure 5) was grown on 150mm-diameter (111) silicon by MOCVD. The top p-GaN layer was removed by

Cap	Magnesium-doped p-GaN	100nm
Cap	GaN	30nm
Barrier	AlGaN	20nm
Channel	Undoped GaN	1µm
Buffer	Carbon-doped GaN	2µm
Buffer	AlGaN/GaN superlattice	1µm
Seed	AlN	
Substrate	Silicon (111)	150mm diameter

Figure 5. III-nitride hetero-structure.

Figure 6. Schematic diagram of AlGaN/GaN HFETs with multi-level metalization



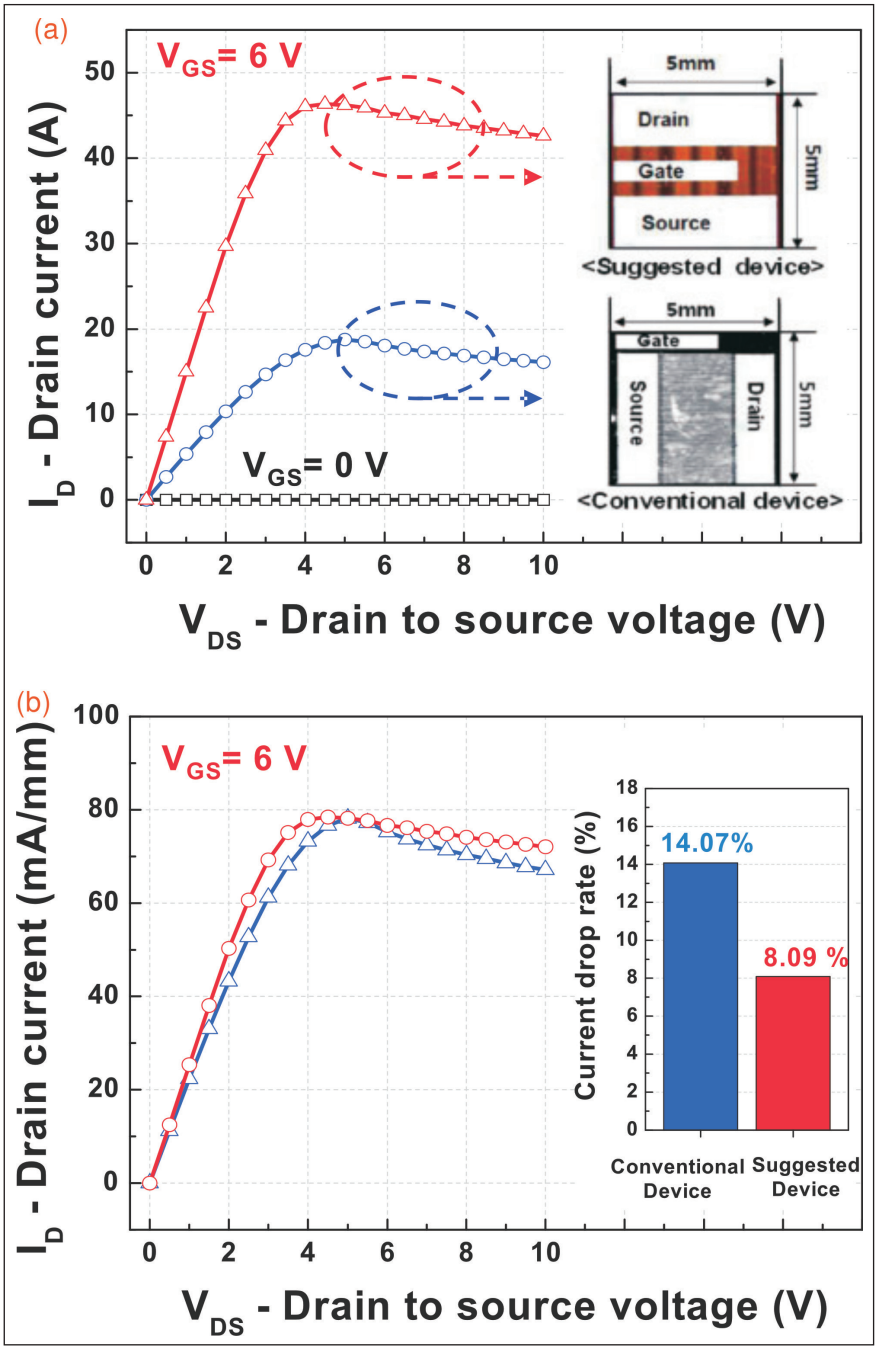


Figure 7. (a) Output power characteristics and (b) current drop ratio of AlGaN/GaN HFETs with multi-level metalization in comparison with conventional HFETs having same chip size.

selective inductively coupled plasma reactive-ion etch except in the gate region of the device. Further etching created device-isolation mesas. Ohmic source/drain electrodes consisted of annealed titanium/aluminium/palladium/gold (Ti/Al/Pd/Au). The gate electrode was nickel/gold (Ni/Au). PECVD silicon nitride was used to passivate surface states.

The first metal layer consisted of Ti/Al lines, deposited after etching via holes in the silicon nitride to make contact with the devices (Figure 6). Further metal layers were separated by photosensitive polyimide (PSPI). The intermetal dielectric (IMD) was spin-coated onto the wafer at 3000 rotations per minute and soft-baked at 120°C for 3 minutes. The material was patterned with via holes using mercury lamp 365nm i-line UV light and development, followed by hard-baking at 140°C for 3 minutes. Curing was carried out at 320°C for 100 minutes in nitrogen atmosphere.

The second metal layer of Ti/Al lines was deposited on the IMD with contacts through the via holes. A further layer of IMD was applied and patterned with via holes. This final IMD layer was treated with oxygen plasma to improve the adhesion between the IMD and the final Ni/Ti/Au source, gate and drain bonding pads.

The researchers comment: "In this structure, the size of the chip is significantly smaller than those of conventional devices due to the location of the bonding pad region directly on top of the active device area."

The normally-off transistors had a threshold of +0.8V. With 6V gate and 4V drain bias, the maximum drain current was 46.3A (Figure 7). With 0V gate, the current leakage was 92μA at 600V drain bias. The breakdown voltage for 500μA leakage was 635V. This was slightly lower than the 670V breakdown of a conventional HFET of the same area.

The gate width of the 5mmx5mm multi-level HFET device was 590806μm (4409μmx134), while the 5mmx5mm conventional HFET gate width was 250800μm (2200μmx114).

The maximum drain current of the conventional HFET was 18.4A with the same biasing as for the multi-level device. The researchers explain: "The maximum drain current, which is related to the output power, for the multi-level-metalization-structured HFETs is 240% higher because the multi-level metalization structure can increase the size of the active area for the same chip size."

As drain bias increased to 10V, self-heating effects reduced the drain current with 6V gate potential 14.07% in the conventional device and 8.09% in the multi-level structure. Self-heating increases phonon scattering and hence reduces carrier mobility in the two-dimensional electron gas channel. The reduced drain current fall off at 10V in the multi-level HFET thus indicates improved heat dissipation. The researchers suggest that this was due to generated heat being transferred from the active area to the surface through the conductive Al via-holes. ■

The author Mike Cooke is a freelance technology journalist who has worked in the semiconductor and advanced technology sectors since 1997.