High-mobility channels and moving beyond silicon

A number of significant changes are seemingly converging on 7nm — lithography, III-V NMOS, Ge PMOS? Here we focus on InGaAs NMOS research.

Reports from February's 2015 IEEE International Solid-State Circuits Conference (ISSCC) in San Francisco suggest that Intel plans to move away from silicon transistors at the 7nm technology node, which is expected to begin around 2018. Intel's existing leading-edge technology is 14nm, producing the 'Broadwell' micro-architecture. The next step will be 10nm, around 2016–17, implemented with more silicon technology.

The question is what does "moving away from silicon" mean? It is widely expected to involve III-V materials and indium gallium arsenide (InGaAs) in particular. These materials have higher mobility — meaning that the carrier drift velocity is higher for a given applied field. The aim of applying high-mobility materials is to achieve denser, faster ICs consuming less power.

InGaAs channels cover the n-channel side of complementary metal-oxide-semiconductor (CMOS) transistors circuits. However, the p-side may be some form of germanium that is chemically related to silicon in the group IV of the periodic table. Suggested alternatives include tin–germanium (IV–IV) or indium gallium antimonide (III–V) alloys. Using two different materials increases complexity and cost, risking development delays.

It is a matter of pride for Intel to stay on the 'Moore's Law' course of shrinking devices by 0.7x every two years — this would give the sequence 14nm–10nm–7nm corresponding to the years 2014–2016–2018. However, the path in recent years has not been simple — Intel delayed its 14nm introduction for several months as a result of reported "manufacturing issues".

Apparently one of these issues was an increase in the number of masks used in photo-lithographic processing, reducing the 'learning rate' in development toward higher yield. This is presumably related to the problem of using 193nm ultraviolet radiation to image deep-subwavelength 14nm features. Over the years, subwavelength lithography has developed various work-arounds to improve resolution, such as optical proximity correction, phase-change masks, immersion in high-refractive-index liquids, and multiple exposures (the cause of the increase in mask number?).

Although extreme ultraviolet lithography (EUVL, with an expected wavelength of ~13nm) has been in development since before 2000, it has been delayed from its initial target of imaging 100nm devices (~2004) and is now not expected to be implemented before the 7nm node. The main problem seems to be with light source power, but there are also infrastructure concerns arising from the different ways that EUVL masks work.

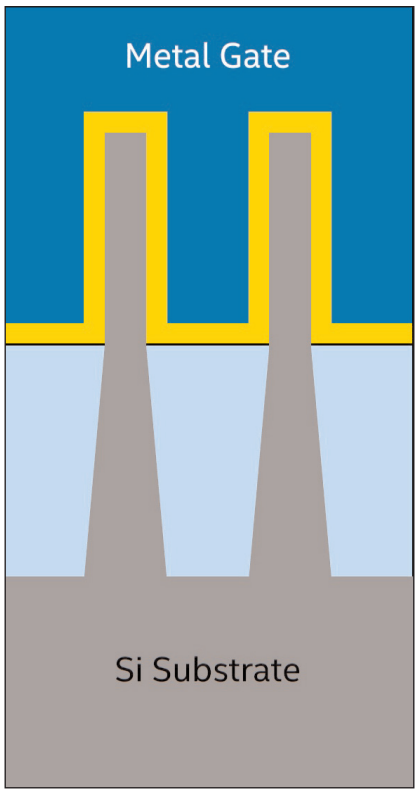

Figure 1. Schematic of Intel 14nm finFET.

Despite the problems, Intel claims that its 14nm technology resulted in a better-than-the-trend drop in cost per transistor. Pilot 10nm devices are reported to be 50% faster than 14nm devices, and the company does not expect any delays.

At first sight it may seem strange that 14nm was delayed, since it is Intel's second generation of tri-gate fin field-effect transistor (finFET, Figure 1). These devices use a series of fins to allow the gate electrode to wrap around the channels, giving increased electrostatic control over traditional planar structures with the applied field coming from just one side.

Intel's first-generation tri-gate was 22nm for the 'Ivy Bridge'/'Haswell' micro-architectures (2012–13). Other companies are due to move to the tri-gate structure at 14nm (Figure 2).

The introduction of InGaAs or some other III–V material channels poses a number of challenges. The first is producing a workable technique for creating InGaAs on 300mm substrates — which are vital for mass production, and this means silicon (since there is no other crystal material available at these diameters).

In 2013, nanoelectronics R&D center Imec of Leuven, Belgium produced InGaAs finFETs on 300mm silicon

wafers with a view to 7nm production. The Imec technique uses wafers with silicon fins that are replaced with InGaAs/InP fins. The European research center has also developed a similar germanium fin-replacement process.

Other groups are working on techniques where InGaAs is grown on much smaller indium phosphide substrates (up to 100mm diameter) and transferred to 300mm silicon by direct wafer bonding. However, this adds process complexity and, hence, cost.

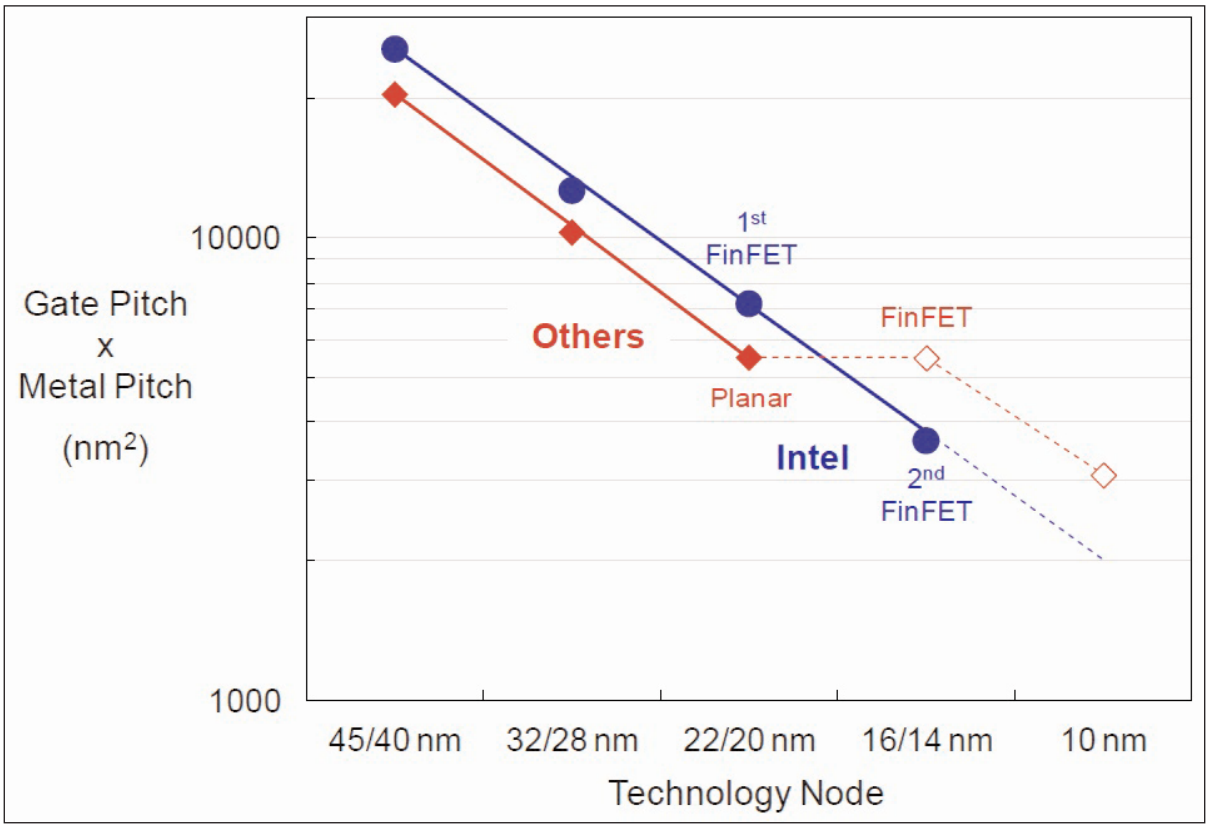

Figure 2. Intel's assessment of transistor scaling for the recent past and near future.

Further aspects of InGaAs transistor fabrication also need work, such as the source/drain contacts of many experimental devices being too large for 7nm and using materials not suitable for a silicon environment.

Boosting swing and transconductance

Researchers based in USA and South Korea have claimed a record combination of subthreshold swing (82mV/decade, 0.5V drain bias), transconductance (1800μS/μm) and on-current (0.41mA/μm) for a tri-gate quantum well InGaAs MOSFET [Tae-Woo Kim et al, IEEE Electron Device Letters, published online 20 January 2015]. The team was based at Sematech Inc in the USA, KANC in South Korea, and GLOBALFOUNDRIES in the USA.

The III-V epitaxial structure was grown on semi-insulating indium phosphide by molecular beam epitaxy (MBE) — see Figure 3. A multi-layer cap was used to control the side spacing, L_{side}, in the combined wet/dry recess etch (Figure 4). Patterning consisted of two electron-beam lithography processes to achieve the desired fin width and gate length. The fin width and height were 30nm and 20nm, respectively.

The 80nm gate length was determined by an opening in a silicon dioxide (SiO_2) layer. The gate insulation consisted of 0.7nm aluminium oxide (Al_2O_3) and 2nm hafnium dioxide (HfO_2) deposited by atomic layer deposition (ALD).

The authors present a benchmark chart of transconductance ($g_{m,max}$) versus subthreshold swing (S) to support their record claim (Figure 5).

Buried yttrium oxide insulator

Korea Institute of Science and Technology has presented what it says is the first demonstration of InGaAs-on-insulator ($In_{0.53}Ga_{0.47}As$-OI) transistors with buried yttrium oxide (Y_2O_3 BOX) layer [SangHyeon Kim

Cap	n^+-$In_{0.53}Ga_{0.47}As$	20nm
Cap	InP	2nm
Cap	n^+-$In_{0.53}Ga_{0.47}As$	20nm
Barrier	InP	1nm
Channel	$In_{0.53}Ga_{0.47}As$	20nm
Back barrier/buffer	$In_{0.52}Al_{0.48}As$	300nm
Substrate	InP	

Figure 3. Epitaxial structure for InGaAs MOSFET.

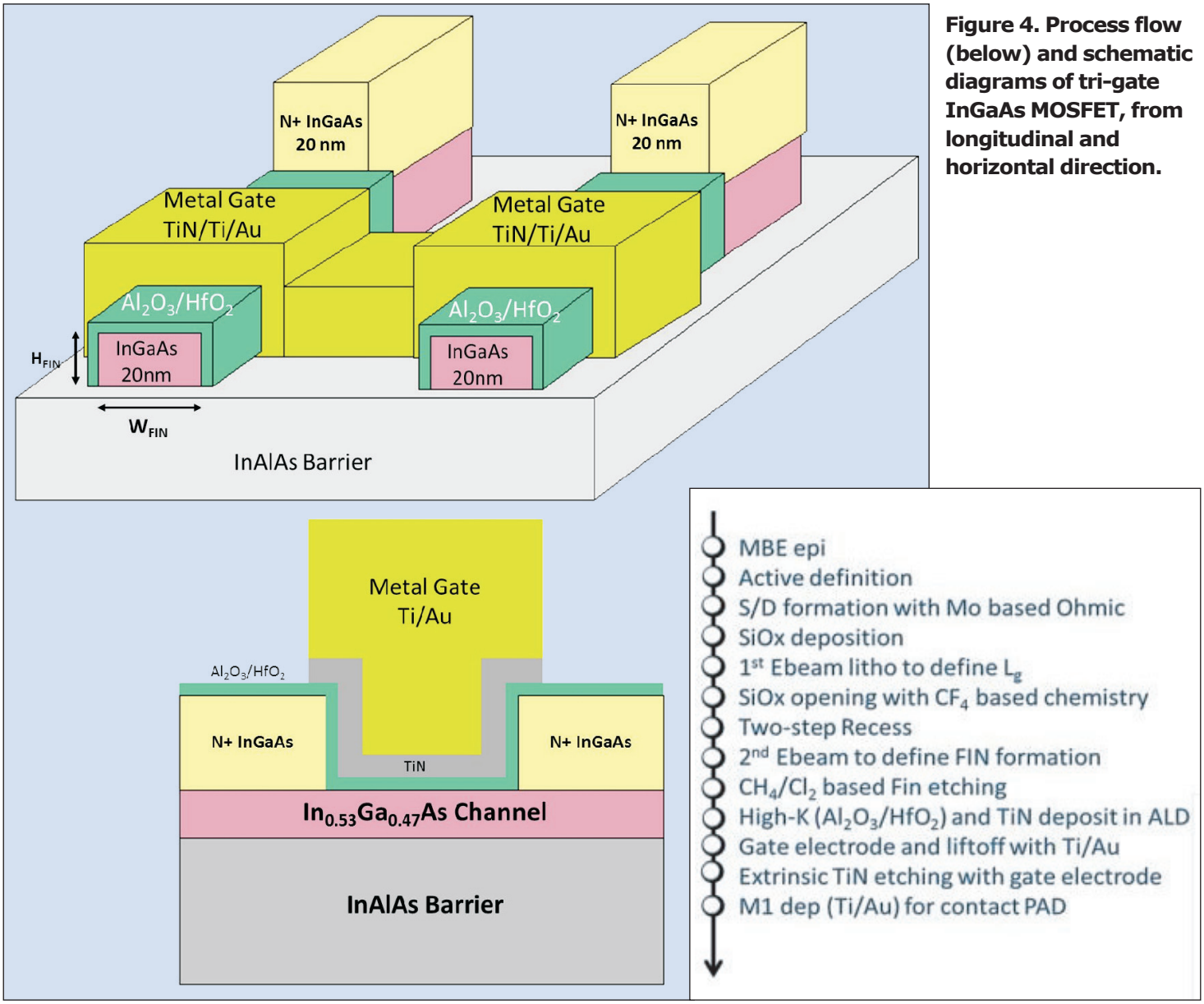

Figure 4. Process flow (below) and schematic diagrams of tri-gate InGaAs MOSFET, from longitudinal and horizontal direction.

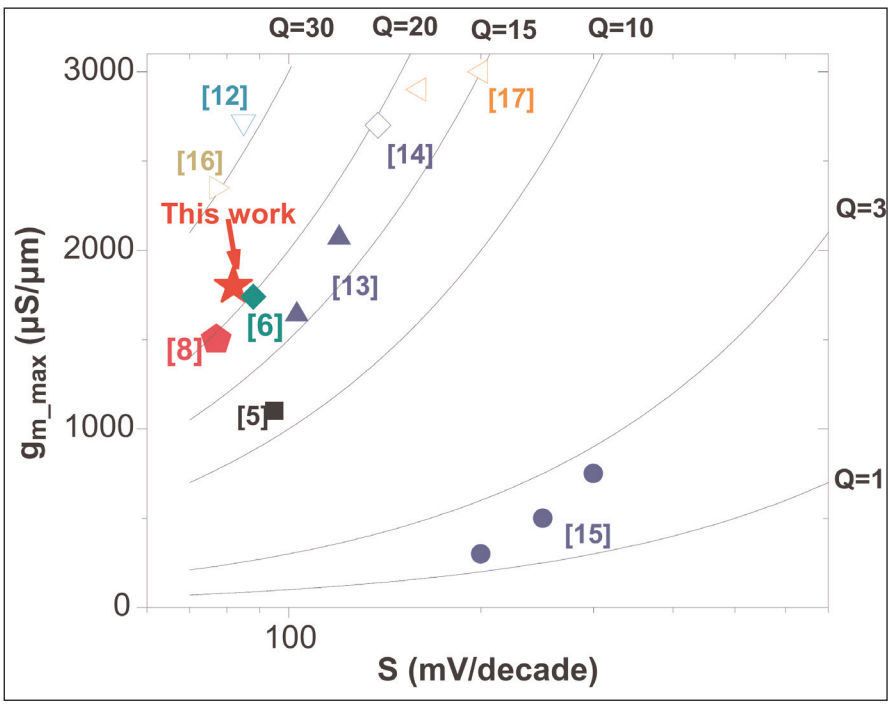

Figure 5. Maximum transconductance versus subthreshold swing, comparing with other reports. Q is $g_{m,max}/S$. Filled symbols are for III-V non-planar MOSFETs and open symbols are for planar MOSFETs. In all cases, the drain bias is 0.5V.

et al, IEEE Electron Device Letters, published online 31 March 2015].

The researchers see InGaAs-OI as a promising alternative to more complicated tri-gate devices. The use of Y_2O_3 should enable reduced equivalent oxide thickness (EOT) compared with aluminium oxide, on the basis of a higher dielectric constant (16 versus 9–12). Reduced EOT brings the gate effectively closer to the channel, improving electrostatic control.

A simple MOS back-gate stack transistor was constructed by layer transfer of InGaAs

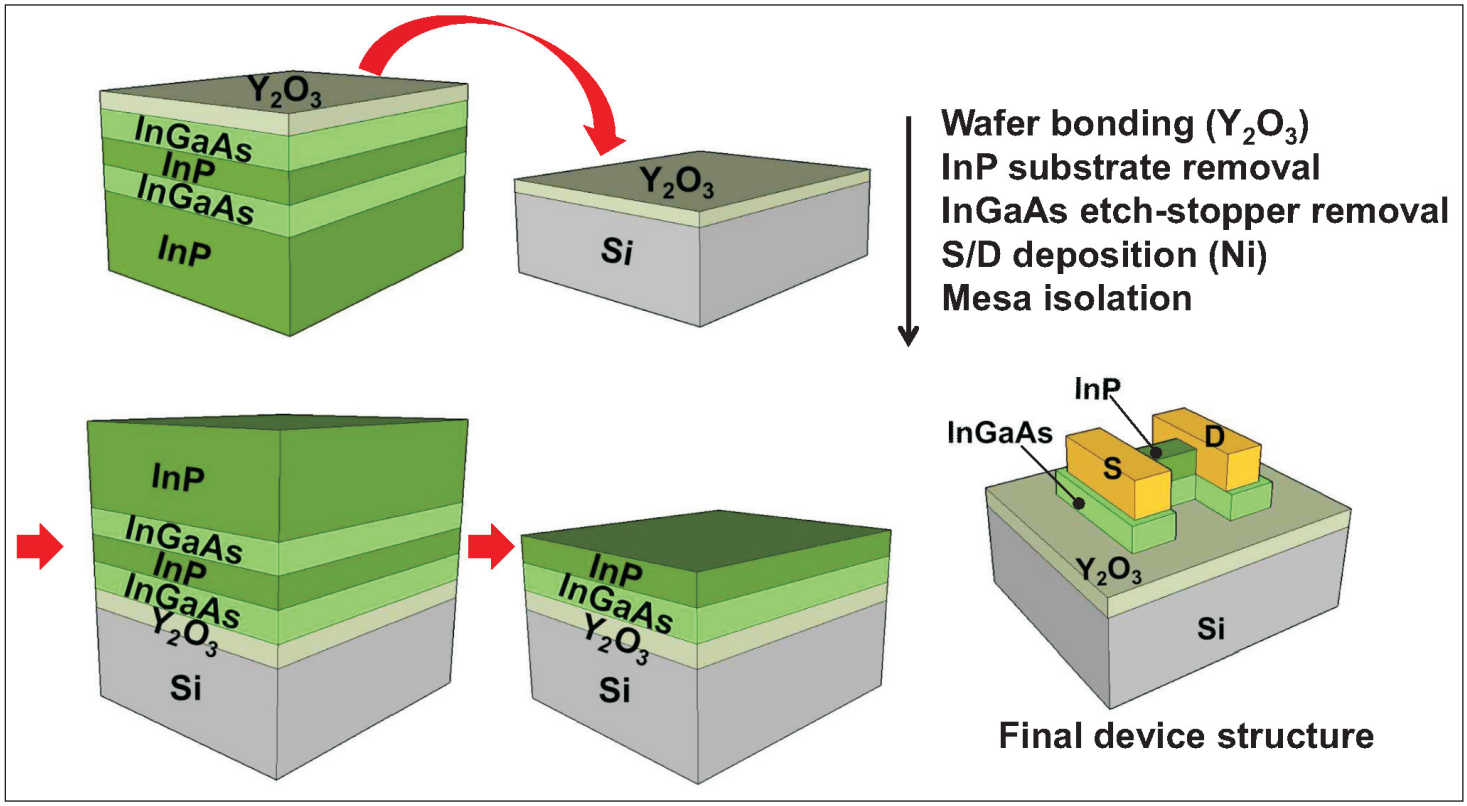

Figure 6. Fabrication process for InGaAs-OI on Si wafer by direct wafer bonding and schematic of final device.

from its InP growth substrate to silicon with a Y_2O_3 buried layer (Figure 6). The InGaAs surface was prepared by native oxide removal and passivation with acetone, ammonium hydroxide and ammonium sulfide solutions. The clean surface was covered with 10nm of Y_2O_3 produced through electron-beam evaporation. The silicon target substrate was also covered with 10nm of Y_2O_3, after cleaning with hydrofluoric acid.

The wafer bonding was achieved with hand pressure in air. The InP growth substrate and an InGaAs sacrificial layer were removed with hydrochloric and phosphoric acid wet etching. Nickel/gold was used for the source and drain electrodes. An InP etch-stop layer was selectively removed from the source and drain areas, but left in place over the channel region to reduce surface effects, which can impact effective mobility.

The final device was subjected to rapid thermal annealing (RTA) at 300ºC. The gate length was 2μm and the body (channel) thickness was 10nm. The subthreshold swing was 90mV/decade, described by the researchers as "very low" in view of the relatively large EOT.

The effective mobility was enhanced by a factor 2.5x over the value for silicon-based devices, even without annealing (Figure 7). Annealing at 300ºC increased the effective mobility to 2000cm^2/V-s. These first results should be improvable with process optimization, say the researchers.

The interface trap density extracted from the subthreshold behavior was 1.1x10^{12}/eV-cm^2, comparable with values from MOS capacitor measurements. These capacitor structures were produced on InGaAs/InP substrates with 10nm Y_2O_3 dielectric, and top and bottom electrodes of platinum/gold and nickel/germanium/gold, respectively. Post-metal annealing at 350ºC reduced interface trap densities to as low as 4x10^{12}/eV-cm^2 near the conduction-band edge, according to capacitance–voltage measurements. The hysteresis was 15mV. ■

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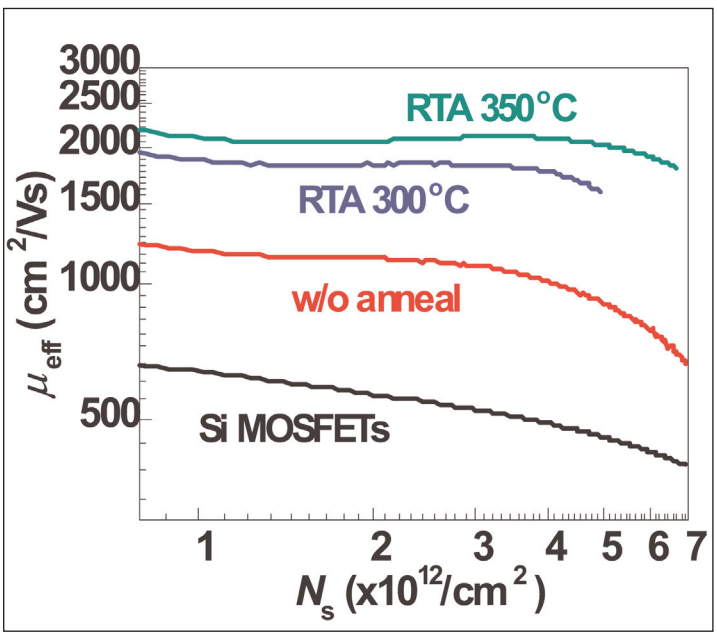

Figure 7. Effective mobility (μ_{eff}) characteristics of InGaAs-OI transistors produced with various annealing temperatures.