High-pressure anneal for indium gallium arsenide transistors

Process reduces interface and border traps in aluminium oxide/hafnium dioxide gate stacks, improving performance and reliability.

Researchers in the USA and Korea have developed a hydrogen high pressure annealing (HPA) process for aluminium oxide/hafnium dioxide (Al_2O_3/HfO_2) gate stacks on indium gallium arsenide (InGaAs) quantum wells [Tae-Woo Kim et al, IEEE Electron Device Letters, vol36, p672, 2015]. The aim of the team, from SEMATECH Inc in the USA, the Korea Advanced Nano Fab Center in South Korea, Poongsan Inc in the USA, and Kyungpook National University in South Korea, was to reduce interface and border traps that adversely affect transistor performance and threshold voltage reliability.

Although the work was carried out on planar metal-oxide-semiconductor capacitors (MOSCAPs) and field-effect transistors (MOSFETs), the researchers add: "We also believe that the HPA process developed in this work would be invaluable for non-planar InGaAs MOSFETs, such as tri-gate architecture, in the sense of recovering the sidewall gate-stack damage through the annealing step."

The researchers see indium-rich InGaAs n-channels as the most promising non-silicon option for continuous scaling down of supply voltages for low-power consumption and boosting transistor performance in future electronics. Although much progress has been made, performance and reliability degradation from interface and border traps continues to be a concern.

Consistent with findings in the InGaAs MOSCAPs, the improvement in the electrostatic integrity of the InGaAs MOSFETs arises mostly from the reduction of D_{it} during the HPA process step

The epitaxial material was grown by molecular beam epitaxy (MBE) on indium phosphide (InP). The quantum well channel consisted of 10nm $In_{0.7}Ga_{0.3}As$ on an indium aluminium arsenide ($In_{0.52}Al_{0.48}As$) barrier layer with inverted silicon δ-doping.

Electrical isolation of the devices was achieved with a wet etch using a solution based on phosphoric acid (H_3PO_4). Ohmic metals for the source–drain contacts were molybdenum/titanium/gold. The gate region was patterned and Al_2O_3/HfO_2 gate insulators and the titanium nitride gate electrode were applied using atomic layer deposition (ALD).

The last stage was the hydrogen HPA, carried out at 300°C under 20 atmospheres pressure for 30 minutes. The tool used was a Poongsan GENI-SYS system (www.poongsan.co.kr/eng/products/high-pressure-annealing-process-system).

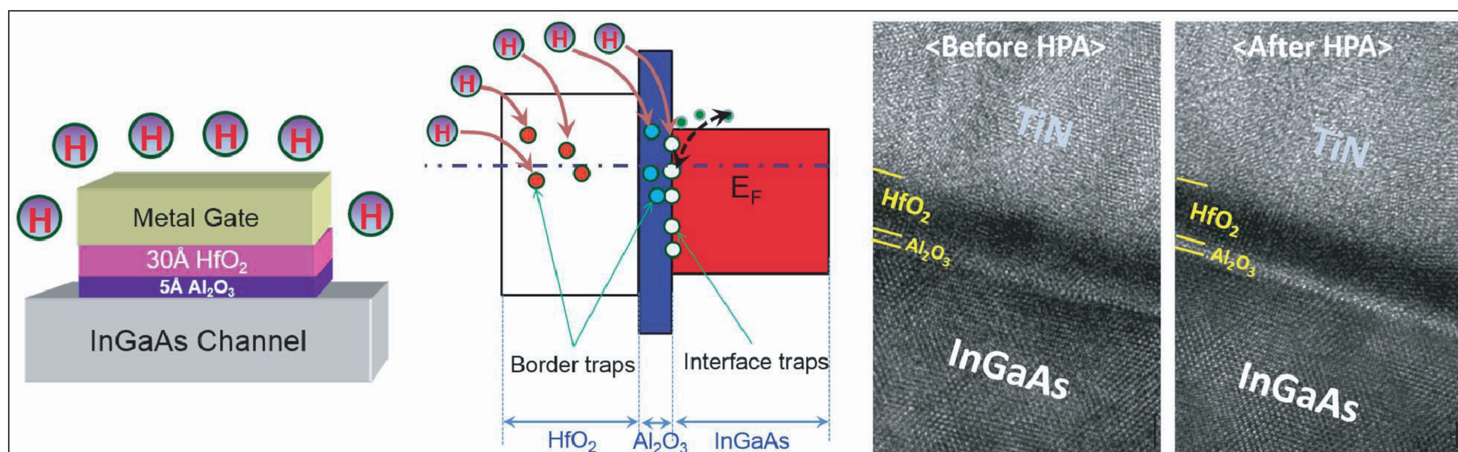

Figure 1. (a) Schematic cross-section for InGaAs MOSCAPs and MOSFETs with HPA, (b) energy-band diagram with interfacial and border traps, and (c) cross-sectional TEM images for Al_2O_3/HfO_2 gate stack before and after HPA.

Table 1. Comparison between InGaAs MOSCAPs and MOSFETs before and after HPA.

	Interface trap density	Capacitance equivalent thickness	Sub-threshold swing	Drain-induced barrier lowering	On-resistance
Before HPA	2.0×10^{12}/eV-cm^2	1.9nm	130mV/decade	68mV/V	540Ω-μm
After HPA	1.1×10^{12}/eV-cm^2	1.8nm	105mV/decade	20mV/V	520Ω-μm

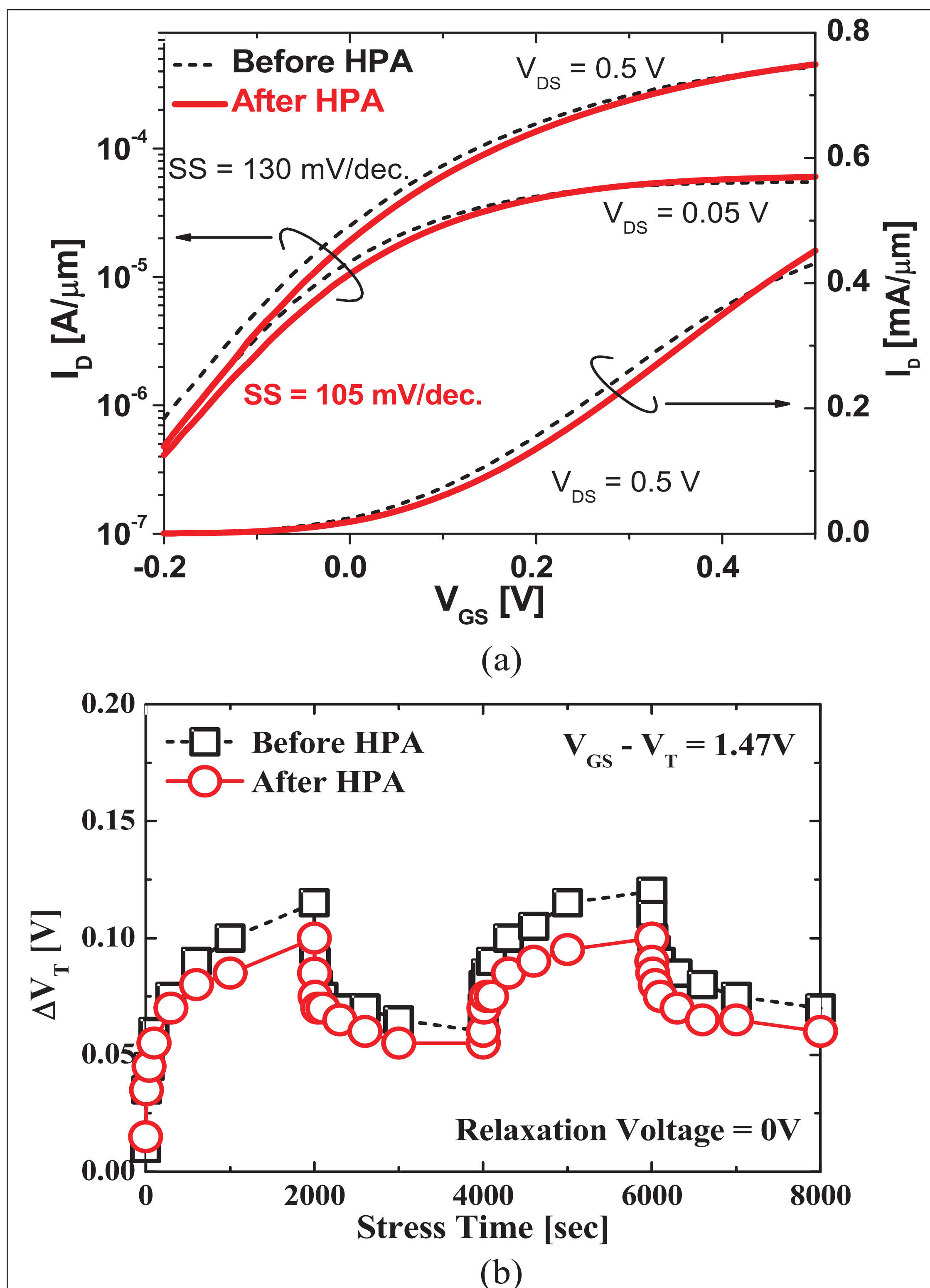

Figure 2. (a) Subthreshold (left) and transfer (right) characteristics of MOSFETs, and (b) ΔV_T profile as a function of iteration of constant voltage stress before (dashed line) and after (solid line) HPA.

The researchers say, on the basis of the capacitance–voltage measurements, that the anneal was effective in reducing border traps. Also, the interface trap density (D_{it}) was reduced by more than 30%, indicating effective passivation (Table 1).

The performance of MOSFETs with 50nm gate length showed reduced subthreshold swing and drain-induced barrier lowering from the anneal process that the researchers describe as "remarkable" (Figure 2a). The researchers comment: "Consistent with findings in the InGaAs MOSCAPs, the improvement in the electrostatic integrity of the InGaAs MOSFETs arises mostly from the reduction of D_{it} during the HPA process step in this work."

Constant voltage stress (3.47MV/cm field) reliability tests showed reduced threshold voltage shift (ΔV_T) from annealed devices (Figure 2b). This was attributed to the reduction in border traps. ■

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