GaN-on-Si large-signal performance beyond 40GHz

Maximum output power density of 2W/mm with power-added efficiency up to 18.5%.

Researchers in Switzerland and the USA have reported the first large-signal performance for a gallium nitride on silicon (GaN-on-Si) high-electron-mobility transistors with output power density of 2W/mm and associated peak power-added efficiency (PAE) of 13.8% (peak 18.5%) at 40GHz without field plates [Diego Marti et al, IEEE Electron Device Letters, published online 9 August 2012]. The researchers also claim the highest cut-off frequencies to date for fully passivated AlGaN/GaN HEMTs on silicon substrates.

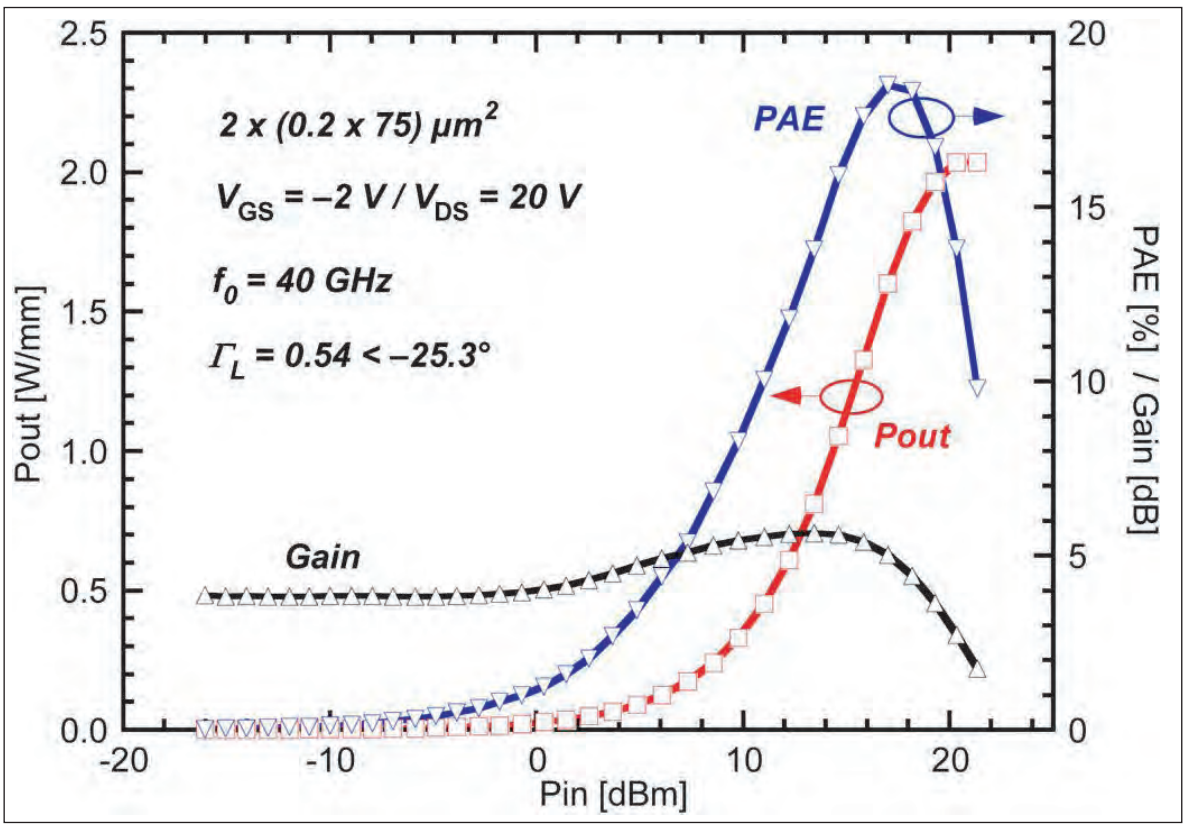

Figure 1. Power sweep of 200nm-gate HEMT at 40GHz at bias conditions of –2V gate and 20V drain. The device showed a maximum output power of 2.05W/mm and a peak PAE of 18.5%.

Four of the researchers are with the Millimeter-Wave Electronics Group, ETH Zürich, and one other is with Nitronex Corp, the supplier of the nitride semiconductor on silicon layers. The substrate was 100mm float-zone refined Si (111) that had a high resistivity (10kΩ-cm). The layers consisted of: a nucleation/transition layer, a 1.7μm GaN buffer, a 1nm aluminium nitride (AlN) spacer, a 17.5nm AlGaN barrier, and a 2nm GaN cap. This resulted in a material with improved mobility of 1500cm^2/V-s and a crack-free surface.

The transistors were formed with 850°C annealed titanium/aluminium/molybdenum/gold ohmic source–drain contacts, mesa isolation, a recessed nickel/platinum/gold T-gate (200nm high, 500nm wide) in the center of the source-drain gap, 75nm silicon nitride passivation, and titanium/gold contact pads.

A range of HEMTs were produced (Table 1). For example, a HEMT with a 100nm gate length in a 1μm source-drain gap had a maximum drain current of 1.05A/mm at 2V gate potential and a maximum transconductance of 540mS/mm (for drain bias of 5V and gate potential of –0.5V). The Schottky gate diode leakage was 300μA/mm at –5V gate voltage. The gate–drain breakdown (1mA/mm) occurred at 29V.

Pulsed measurement to assess current-collapse/gate-lag effects showed little dispersion, indicating low-damage impact from the processing despite the deep recessing used. The researchers comment: "The drain lag is moderate and can be attributed to the surface SiN passivation as well as the improved channel confinement associated with the AlN spacer."

Small- and large-signal radio frequency measurements (0.2–40.2GHz) were carried out. The small-signal investigations of a 75nm gate-length device resulted

(1) MEASURED AT PEAK f_T BIAS; (2) MEASURED AT V_{DS} = 10 V; (3) MEASURED AT V_{DS} = 15 V; (4) MEASURED AT V_{DS} = 20 V. UNDERLINING MARKS BEST OBTAINED VALUES IN EACH COLUMN

L_G (nm)	SD (μm)	f_T/f_{MAX} (GHz) (1)	f_T/f_{MAX} (GHz) (2)	Max(P_{out}):PAE (W/mm : %)	Max(PAE):P_{out} (% : W/mm)
75	1	**152/148**	88/**158**	1.00 : 5.3 (3)	14.3 : 0.70 (2)
75	2	137/132	75/117	1.30 : 8.0 (3)	14.6 : 0.85 (2)
100	1	121/146	95/145	1.56 : 12.9 (3)	**25.0** : 0.75 (2)
100	2	122/134	**96**/133	1.38 : 7.8 (2)	23.7 : 0.90 (2)
100	4	110/75	93/132	0.95 : 1.3 (4)	6.0 : 0.55 (4)
200	1	45/48	63/104	1.60 : 5.0 (4)	19.0 : 0.95 (2)
200	2	75/118	60/118	**2.05** : 13.8 (4)	18.5 : 1.80 (4)
200	4	70/110	57/109	1.55 : 6.5 (4)	22.8 : 0.85 (2)

Table 1. Large- and small-signal parameters.

in cut-off frequencies (f_T) of 125GHz and maximum oscillation (f_{max}) of 145GHz before de-embedding.

Making de-embedding corrections at a drain bias of 2.6V and gate bias of –0.5V, using extrapolations of Mason's unilateral gain parameter, gave f_T of 152GHz and $f_{max(U)}$ of 149GHz. The researchers comment: "This f_T is the highest value ever reported for any GaN HEMT on silicon, exceeding the previous record established using AlInN/GaN HEMTs, providing a 42% improvement with respect to our previous 75nm AlGaN/GaN-on-Si devices."

The corresponding results for a gate length of 100nm were an f_T of 120GHz and $f_{max(U)}$ of 140GHz (3V drain, –0.4V gate).

The frequency performance is also maintained at the drain biases needed for large-signal operation. The devices were tested at 40GHz in a set-up with a nonlinear vector network analyzer (Agilent PNA-X NVNA) source and load-pull. A 200nm gate–length device with 2μm source-drain gap had maximum power output density of 2.05W/mm and corresponding power-added efficiency (PAE) of 13.8%. At a lower power output density of 1.8W/mm the PAE peaked at 18.5% (Figure 1). The gate leakage was 0.3mA/mm during operation.

In general, the longer gates give better large-signal performance (Table 1). "The results confirm GaN-on-Si technology as a promising contender for low-cost millimeter-wave power electronic applications," the researchers write.

Although better performance can be obtained on much more expensive silicon carbide substrates, there is much interest in GaN-on-Si for wider application in high-frequency high-power electronics. According to the researchers, there have been no reports of large signal for GaN-on-Si beyond 20GHz until now. However, low-noise performance has been reported in recent weeks (see www.semiconductor-today.com/news_items/2012/AUG/IEMN_090812.html). ■

http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=6264085

www.nitronex.com

Author: Mike Cooke