Driving 'on-silicon' solutions in lighting, power electronics & PVs

Translucent describes how it grows rare earth oxides using a solid-source epitaxial technique to enable high-quality MOCVD of not only GaN FETs and LEDs but also germanium CPV cells on silicon, leveraging the economies of scale of large-diameter wafers.

In the evolution of today's electronics industry, the demands for lower power, faster performance and more economic solutions continue to exert pressure on materials engineering. Many companies are now exploring how they can more fully utilize mature, robust manufacturing technologies to achieve these goals. 'On-silicon' solutions, which harness standardized technology on low-cost silicon wafers, are now beginning to be not only topical and strategic but also tactical. Indeed, a number of companies have upgraded their R&D programs to full-blown advanced manufacturing programs, targeting production within the next year.

Many of the fast-growing applications such as lighting and power electronics have moved to gallium nitride (GaN) as a vehicle for next-generation devices. In order to keep device costs under control, many major manufacturers are developing GaN-on-silicon (GaN-on-Si) technologies that would be compatible with 200mm wafer fabrication lines that are available in the silicon industry.

For example, Bridgelux Inc of Livermore, CA, USA recently announced GaN LEDs on silicon substrates with record luminous efficacy of 160lm/W. Conventional LEDs are made using sapphire or silicon carbide (SiC) substrates, both of which are expensive compared with the cost of silicon substrates. Silicon also enjoys the availability of large-diameter wafers and mature processing technology. Combined, these factors yield a cost reduction of 75%, Bridgelux projects.

As another example, Nitronex Inc of Raleigh, NC, USA (which was founded in 1999 as a spin-off from North Carolina State University) is producing power transistors using its patented SIGANTIC GaN-on-Si process for power devices in order to address the WiMAX, broadband and cellular markets.

In addition to solid-state lighting and power electronics, another industry that can benefit from 'on-silicon' solutions is the concentrated photovoltaic (CPV) solar industry. The CPV market uses high-efficiency multi-junction (MJ) solar cells, typically grown on germanium (Ge) or gallium arsenide (GaAs) substrates. These cells are then placed at the focal point of optically concentrated sunlight, in either large panels or reflecting dishes. In the case of the reflecting dishes — which have undergone nearly two decades of development by Solar Systems in Australia — the sunlight is focused onto a dense array of these highly efficient solar cells to generate electricity. This industry is also following a similar trend: the drive to bring down the cost of MJ solar cells by creating Ge-on-Si solutions at 150mm (and eventually at 200mm). CPV now demands the combination of superior solar cell efficiencies (>40%) with the economies of scale from silicon.

A need common to both the GaN device industry and the Ge device industry is a novel materials solution that would allow an 'on-silicon' platform for entry into the huge silicon infrastructure. Translucent has spent a decade developing a portfolio of rare earth oxide (REO) materials that are lattice matched to silicon in order to yield excellent crystalline results. The work has all been based in the company's facility in Palo Alto, CA, which houses a number of development and production growth reactors, wafer characterization, and a processing line for 100mm wafers. The growth reactors are solid-source based and can provide a suitable surface for growth by metal-organic chemical vapor deposition (MOCVD).

In the case of GaN high-voltage power field-effect transistors (FETs), full FET structures incorporating REO as both the buffer and a high-K gate dielectric can be manufactured with this technology. Already,

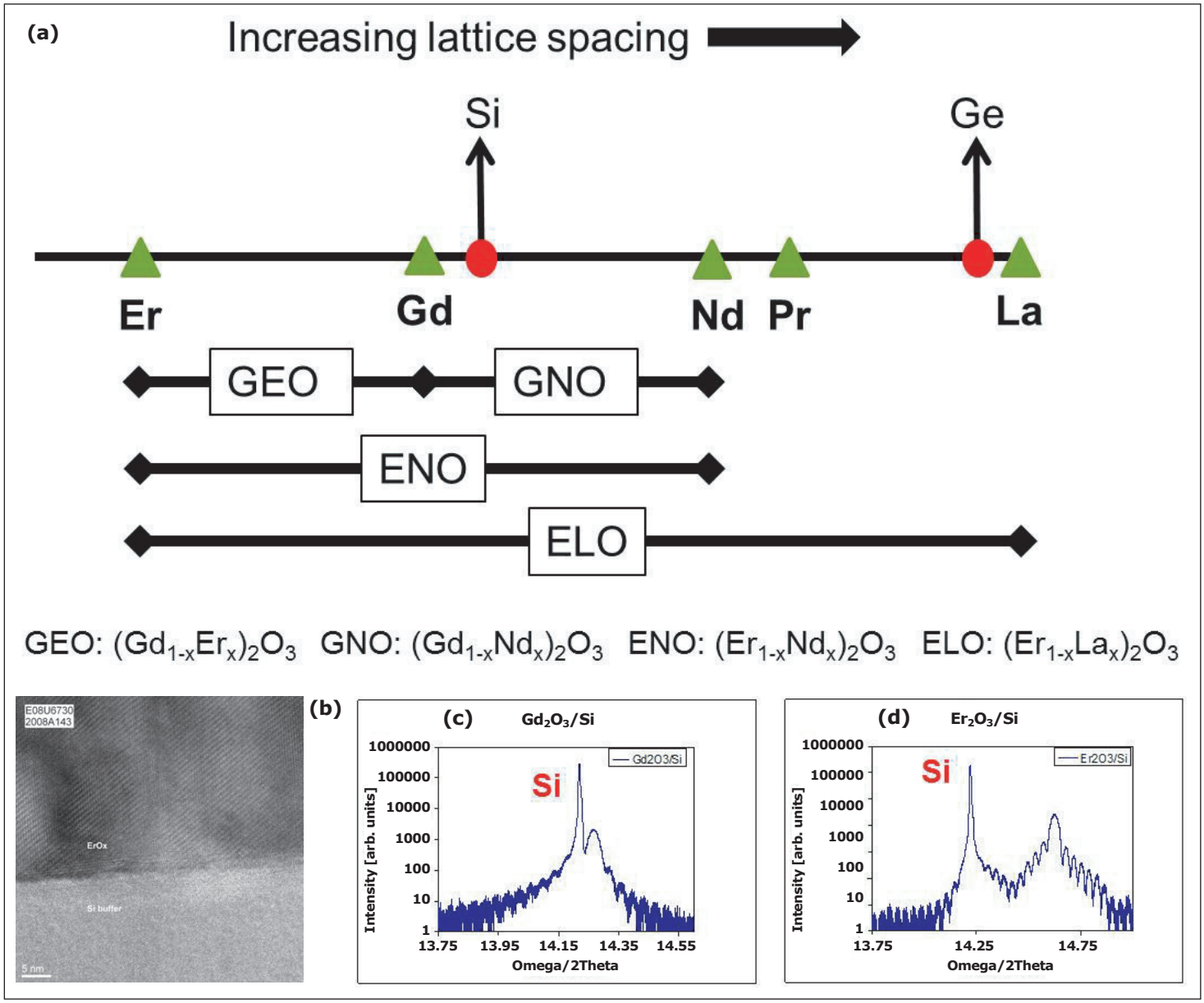

Figure1: (a) Comparison of lattice constants of REOs with relevant semiconductors. (b) TEM image showing the abrupt interface between silicon and Er_2O_3. Similarly, growth of other REOs is possible without interfacial layers formed at the interface region. (c) High-resolution x-ray diffraction of Gd_2O_3 showing well defined Pendellösung fringe, indicating sharp interfaces between oxide and silicon. (d) Similar XRD pattern for Er_2O_3, showing that oxides with different rare earth elements can be grown on silicon.

GaN-on-Si templates ready for MOCVD device growth for both FETs and LEDs have been grown by Translucent on 100mm- and 150mm-diameter wafers, and scaling to 200mm is expected in 2012. Ge-on-Si for CPV solar has also been demonstrated at 100mm, and is being scaled to 150mm in late 2011.

Rare earth oxides that are grown epitaxially using solid-source techniques exhibit high-quality crystalline forms. A comparison of the sizes of the crystalline unit cell for the various rare earth oxides relative to the major semiconductor material in use today shows why they are a highly relevant material to the industry. The oxides are in fact 'lattice coincident' — each oxide's crystalline unit cell corresponds to two crystalline unit cells of the underlying semiconductor. Figure 1 shows this relationship, along with x-ray diffraction data from one of the binary oxides epitaxially grown on silicon, showing the quality of the epitaxial oxides on silicon.

The accompanying transmission electron micrograph (TEM) shows just how sharp the interface between oxide and substrate is, and how a well engineered process can avoid the formation of interface silicates. Just like traditional III-V semiconductor epitaxy, the oxides can also be grown as ternary compounds, enabling graded structures to be epitaxially produced on silicon. Some of the ternary oxides developed at Translucent include $(Gd_{1-x}Er_x)_2O_3$ and $(Er_{1-x}Nd_x)_2O_3$. These are also shown in Figure 1 as GEO and ENO, respectively.

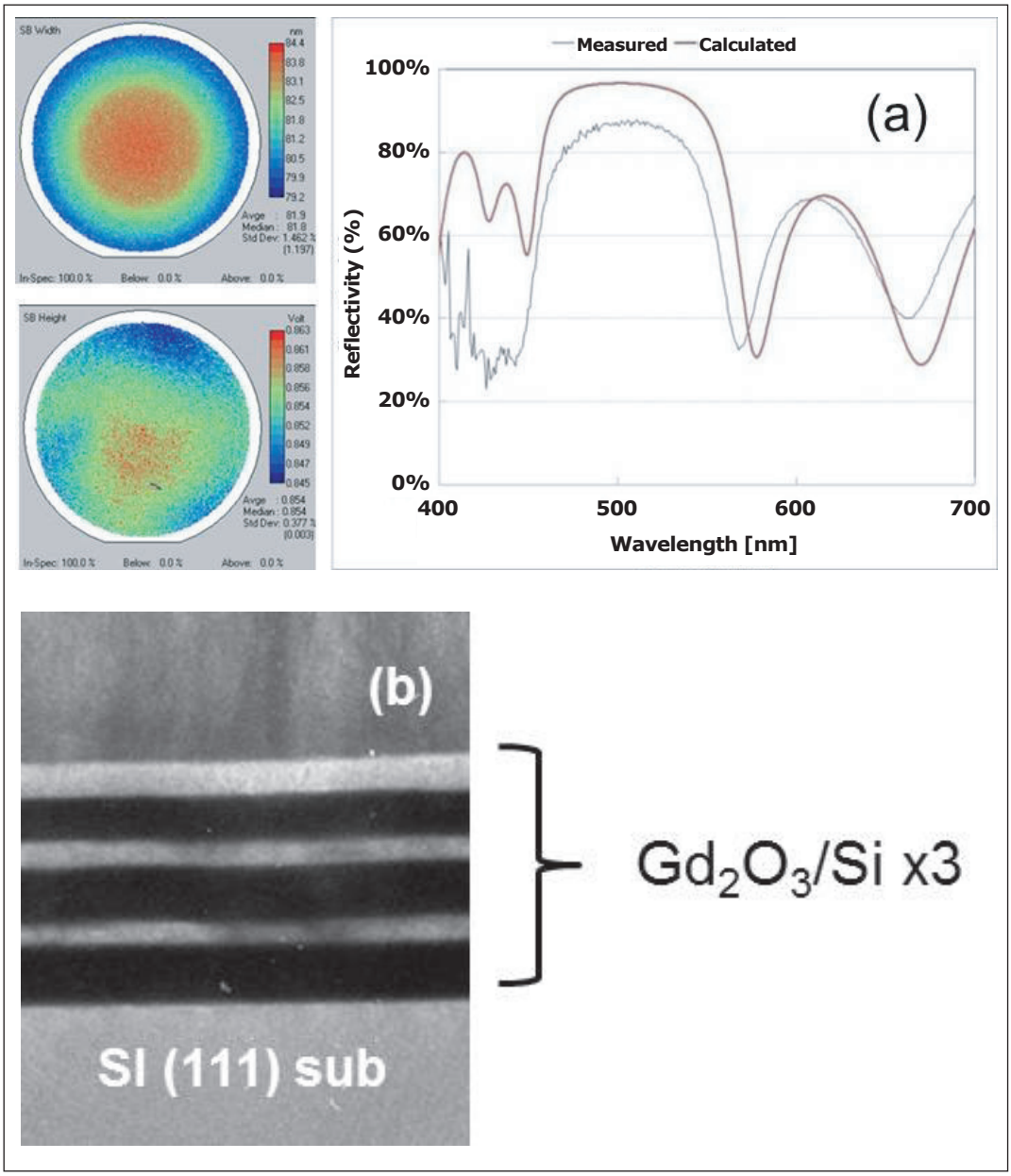

Figure 2 (a) Reflectivity map of DBR structure under white light and reflectivity spectrum of a three-period DBR structure made from oxide/silicon multilayers (black curve), simulation of the experimental data (red curve). (b) TEM image of the DBR mirror on Si(111) consisting of a three-period oxide/silicon stack.

Given its proximity to the lattice constant of silicon, almost all oxide structures start with Gd_2O_3; what is placed on the upper surface is then chosen according to the application. For example, La_2O_3 would be a good choice if the next layer was to be Ge. This ability to grow a high-quality oxide followed by an epitaxial semiconductor layer is the core building block in the production of compliant/template substrates.

It is also the reason why distributed Bragg reflector (DBR) structures can be produced epitaxially on silicon substrates. With a typical refractive index of n=2.0, the Δn that results from a pairing with silicon (n=4.25) enables large bandwidth reflectors that achieve >85% reflectivity after only 3–4 periods of growth. Figure 2 shows some typical DBR data. For a fuller description, see Translucent's paper from the 9th International Conference on Nitride Semiconductors (ICNS-9), July 2011 (available at www.transclucentinc.com).

These mechanical attributes, combined with a growth process that enables good control of the compositional aspects of the oxides, enabled the development of a family of 'on-silicon' template wafers with good surface compliancy and stress management. The first of these (silicon-oxide-silicon, cSOI) was developed as an alternative to the traditional two-wafer-bonded approach to SOI. Compatible with a commercial foundry-based silicon reactor, the template supported the growth of 10um of silicon via a high-temperature trichlorosilane CVD process. The thermal conductivity of the oxide layers are approximately five times better than that of SiO_2, as verified by the 3ω method. Even with good epitaxial crystallinity, the SOI industry seems to be comfortable with bonded wafers from companies such as SOITEC of Bernin, France.

More recently, the focus at Translucent has turned to III-N-on-silicon for both the solid-state lighting (SSL) and power industries, where the economies of scale available through the use of large-diameter silicon are expected to drive the next advance in the adoption of the nitride technology. In this instance, the role of the template is to utilize materials engineering to control the wafer stress and the nucleation of the nitride material such that the growth of the LED by the traditional MOCVD process is made simpler.

Wafer stress can be engineered through the use of binary and ternary rare earth oxides with different lattice constants. Pre-stressing wafers is an important process to reduce wafer bow, especially on larger-diameter silicon wafers (150mm and 200mm). Currently, companies such as Azzurro Semiconductors AG of Magdeburg, Germany manage to control wafer bow

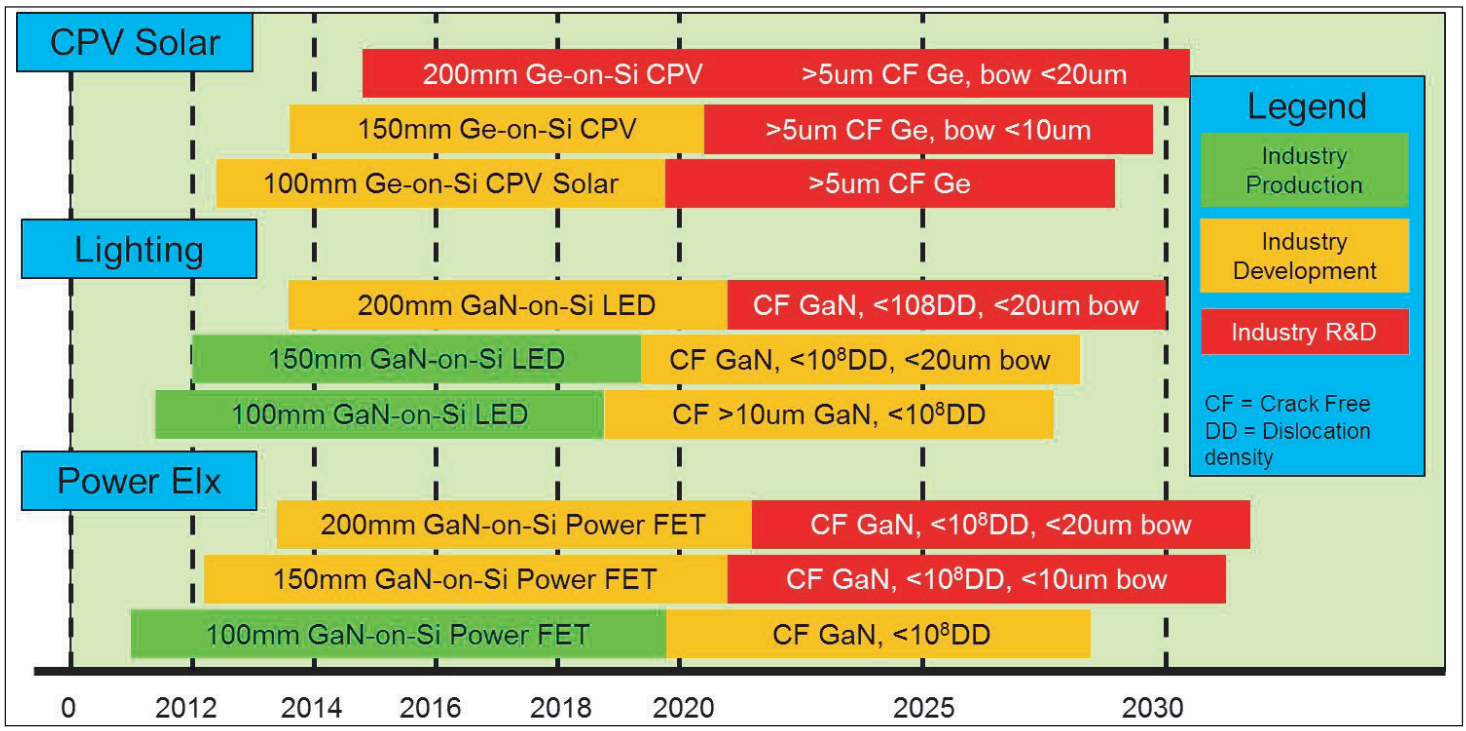

Figure 3 Industry roadmap for 'on-silicon' solutions showing trends towards 200mm silicon wafer sizes.

stress through Ge doping of GaN as well as interlaced layers of low-temperature aluminum nitride (AlN).

A pre-stressed wafer with a simple REO layer that has been engineered to minimize lattice mismatch is an attractive option for large-diameter 'on-silicon' technologies. In this case, REOs provide surface compliancy, stress management, and precise crystalline lattice control of the epitaxial layers to provide a very high quality of template that compares favorably with existing wafer technologies on the market. The REO layers, which are grown using a production-grade solid-source epitaxial reactor designed and constructed by Translucent engineers and scientists, are stable and can withstand the high 1100°C temperatures of an MOCVD reactor. A number of experiments have been performed to verify the integrity and performance of capped REOs at 1100°C for MOCVD reactors. The Translucent reactors derive from molecular beam epitaxy (MBE) designs, however they are modified for production fabrication plants.

The drive towards larger silicon wafers for 'on-silicon' solutions is shown in Figure 3. The industry roadmap shows wafer size trends for three major applications: solid-state lighting, power electronics, and solar CPV. In all applications, the drive to 200mm silicon wafer technology will enable better economies of scale for products.

Key criteria are noted in the roadmap:
(1) crack-free (CF) GaN growth;
(2) defect dislocation density (DD); and
(3) wafer bow.
All these criteria are key merits of success for 'on-silicon' technology. Crack-free GaN implies that the crystal and thermal stress issues are resolved, while low defect dislocation densities are needed to drive higher device performance. Wafer bow becomes an issue on larger wafer sizes and indeed is a by-product of stress induced by the dissimilar epitaxy. Low wafer bow allows for easier handling in silicon fabrication plants, as well as better photolithography during device processing.

In summary, rare earth oxides have been developed to provide excellent quality crystalline templates for GaN and Ge epitaxial growth. Rare earth oxides can alleviate mechanical (stress, lattice mismatch, bowing), thermal (runaway), optical (mirrors), and electrical (gate dielectric, field suppression) issues as well as, importantly, economic issues involving compound semiconductor devices.

The industries that are looking for 'on-silicon' solutions include solid-state lighting and power electronics in the GaN-on-Si field, and CPV solar in the Ge-on-Si field. Even though these industries seem to be the leaders in driving wafer platform economies of scale, other industries are standing by; for example, the vertical-cavity surface-emitting laser (VCSEL) and GaAs electronics industries are watching very closely as the technology scales to 200mm GaAs wafers. So, as industries and product manufacturers demand more cost-effective solutions to fast-moving applications, the future for rare earth oxides looks bright. ■

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