Compounding energy efficiency and performance

IMEC recently held its annual meeting presenting work to the international press. Mike Cooke attended and reports on some of the center's research in relation to compound semiconductors.

With costs increasing across the main branches and tentacles of the semiconductor industry, sharing research costs has become increasingly important. The IMEC research center in Leuven, Belgium has been at the forefront of this trend since 1984.

Until recently, the center has focused mainly on silicon devices in terms of complementary metal-oxide-semiconductor (CMOS) integrated circuit and micro-electro-mechanical systems (MEMs) processing, electronics design and bioelectronics for medical applications. But now, ever increasing demands for CMOS circuitry performance and higher energy efficiency technologies have shifted the focus to compound semiconductor technology in the past few years. These include nitride semiconductors for high-voltage circuits and light emission, thin-film materials for lower-cost photovoltaic solar energy conversion, and bandgap engineering for high-mobility channels in high-speed/low-power CMOS transistors.

Energy efficiency

The main work at IMEC concerning nitride semiconductor application centers on energy efficiency. Philip Pieters, business development director energy at IMEC, reported on research around the power efficiency possibilities arising from use of nitride semiconductors, both in the form of high-efficiency power conversion electronics and light emission. In particular, IMEC wants to use its silicon expertise as a platform for producing such devices cost effectively.

The wide bandgap of nitride semiconductors allows for the emission of visible light, and for power components a high critical breakdown voltage can be achieved. For power electronics, this means that high power density can be achieved with low switching losses.

IMEC has a dedicated III-V processing area that can handle 4-inch substrates. However, the center is working towards using larger-scale facilities such as the 6-inch MiPlaza facility (in Eindhoven, The Netherlands)

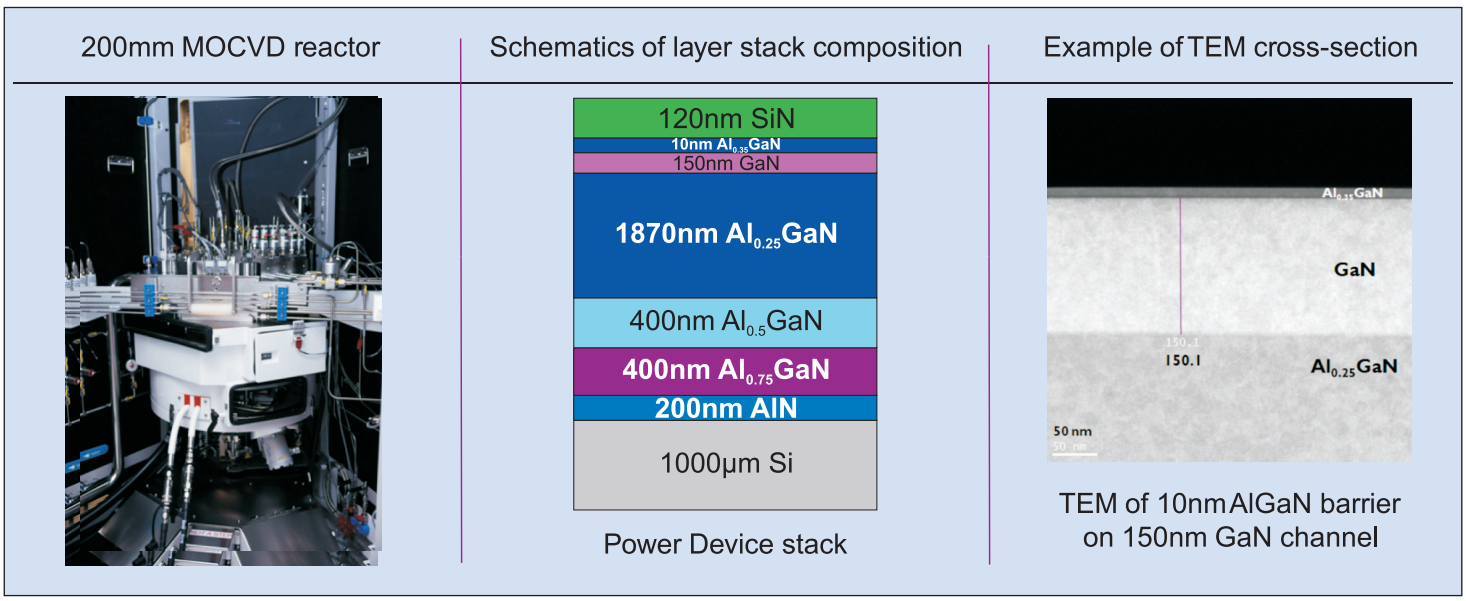

Figure 1. Some IMEC achievements of GaN epitaxial growth on 200mm silicon.

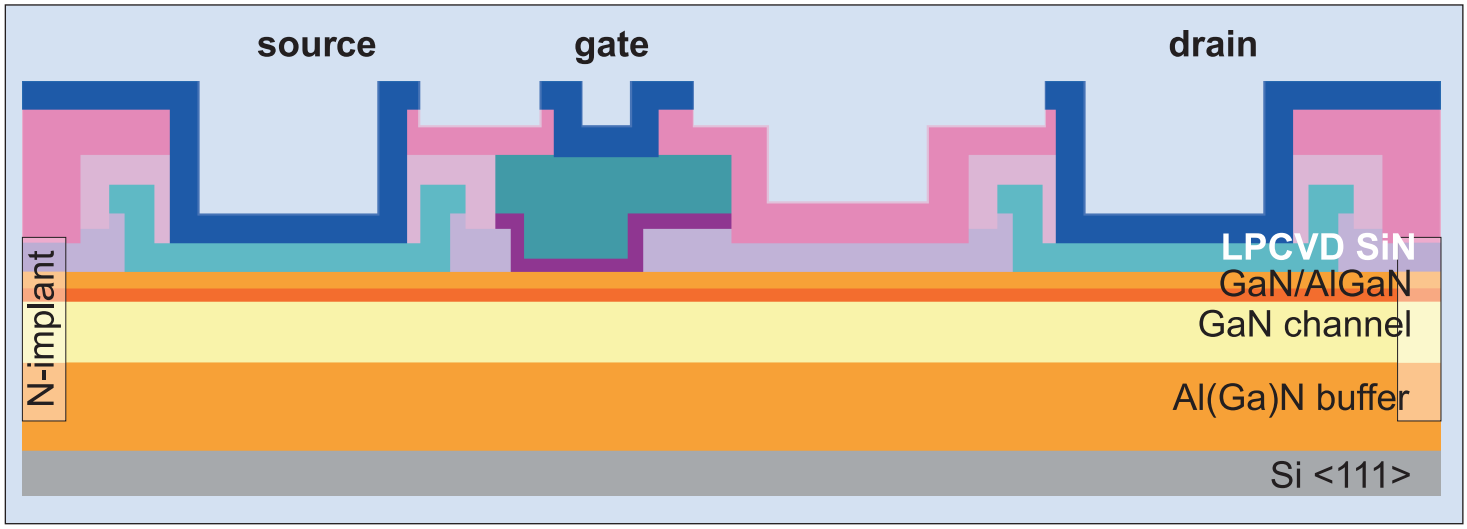

Figure 2. Structure of power devices from silicon-compatible 200mm process.

and its own 8-inch (200mm) pilot line. Indeed, IMEC has produced the first GaN layers on 200mm silicon substrates and has an industrial Applied Materials 200mm MOCVD system installed and operational.

Among the 200mm achievements are complex aluminum gallium nitride (AlGaN) layers for power devices such as high resistive buffer, GaN channel, and single/twin barriers; and, for light-emitters, quantum wells, p-type GaN and AlGaN, and n-type GaN (Figure 1).

Such material has been used to create the first 200mm GaN-on Si-power device (Figure 2) with functional transistors found on the first two pathfinder lots. Also, building up the work in the past year, IMEC has recently (in September 2011) produced fully functional GaN LEDs on 200mm silicon (Figure 3).

The IMEC epitaxy process on silicon has buffer layers that can handle 600V and even voltages beyond 1000V. The center has also previously developed an in-situ nitride passivation that is part of the portfolio of the spin-out company EpiGaN of Hasselt, Belgium, which provides nitride-on-silicon wafers.

In its 4-inch facility, IMEC has developed a process of reference involving 12 masking steps, eight before metal-1. For practical application of the technology, circuit layout and design, simulation, characterization and reliability activities have also been developed.

Solar energy from thin-film photovoltaics

Although thin-film PV constituted less than 20% of 2010's $50–60bn market, this share is expected to increase to 25% in the period up to 2025, according to IMEC's Marc Meuris, team leader novel materials.

While some thin-film PV uses amorphous silicon, it is advantageous in terms of lower material use to employ direct-bandgap material, rather than indirect silicon.

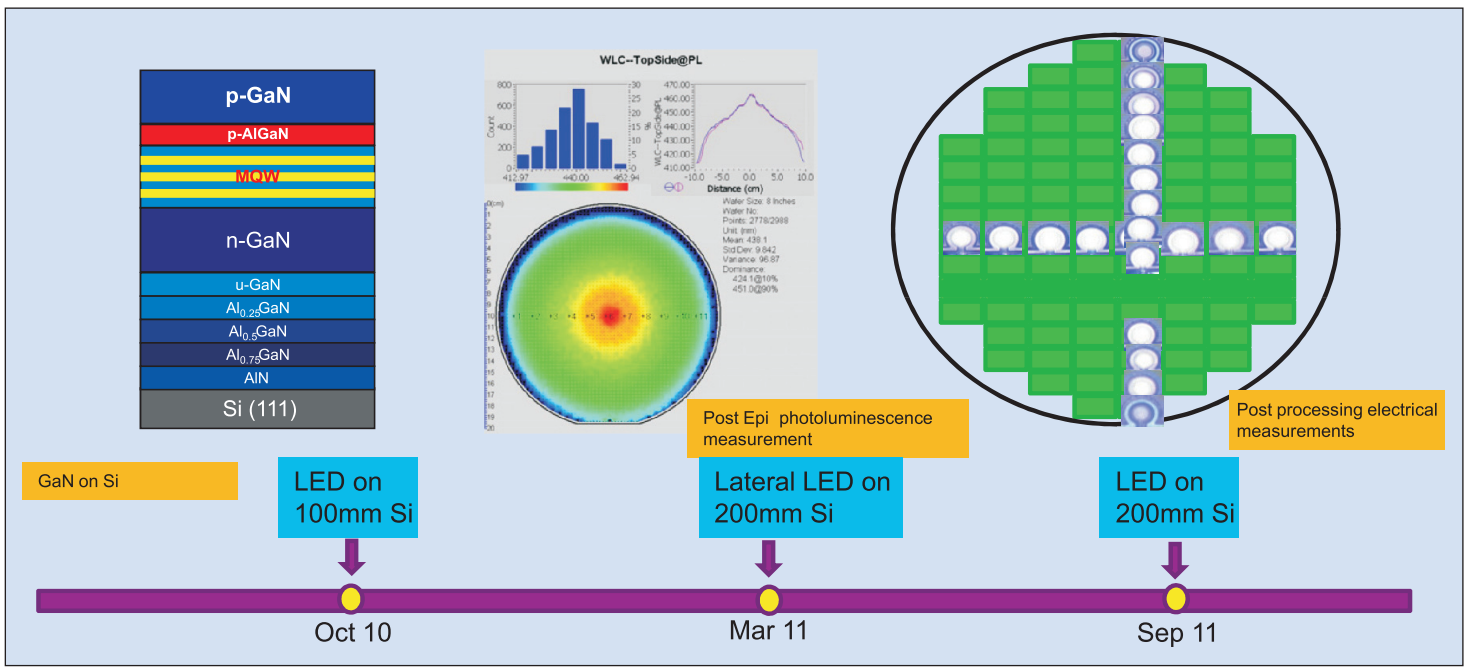

Figure 3. IMEC timeline for fully processed blue GaN LEDs on 200mm silicon.

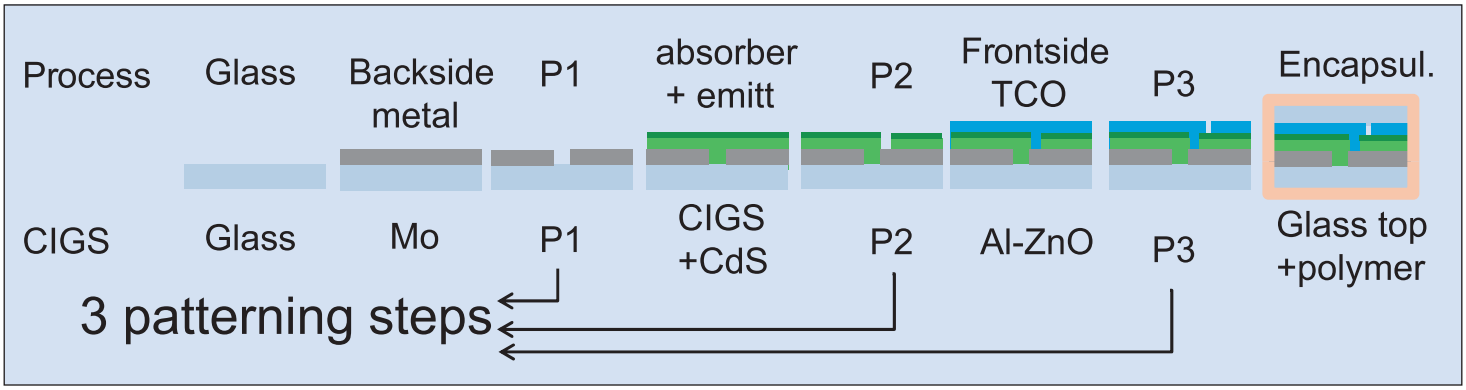

Figure 4. Process flow for conventional thin-film photovoltaics (TF-PV).

Thin-film PV materials can be processed for lower cost using less complicated manufacturing process flows (Figure 4).

Presently, these alternative materials are, for example, cadmium telluride (CdTe) and copper indium gallium diselenide (CIGS). Although these materials have performed well (17.3% laboratory efficiency for CdTe; 20.3% for CIGS), both of these options have price concerns, centering on tellurium and indium supply. Also, the cadmium-containing compound raises health concerns.

Low-cost alternatives to CIGS are being sought among 'kesterites' materials such as copper-zinc-tin-sulfide/selenides (CZTS) and sulfosalts (e.g. tin-lead sulfide). $Cu_2ZnSnSe_4$ PV devices have recently achieved 10% efficiency. CZTS covers the bandgap energy range 1.0–1.6eV that is needed to create multi-junction cells that respond to solar radiation with a range of wavelengths.

IMEC is focusing on CIGS and CZTS. For CIGS, the center is developing a solution-based solar cell integration flow, while for CZTS the aim is to build up materials expertise.

For the CZTS work, the researchers want to improve both the composition (stoichiometry) and crystal quality control, along with perfecting contamination (passivation, etc) and dopant technologies. IMEC has a molecular beam epitaxy (MBE) system that is due for installation next year (2012) to be used in the CZTS work. In particular, IMEC is seeking two material compositions that can be used to create multi-junction devices that respond efficiently to different bands of the solar spectrum.

The IMEC work receives funding both from its own funding programs and through the European 'Solliance' of TNO (the Netherlands Organization for Applied Scientific Research in Delft), IMEC, the Holst Center in Eindhoven (a joint research initiative of Imec and TNO), ECN (the energy research institute of The Netherlands) and TU/e (Eindhoven University of Technology) for R&D in thin-film PV, situated in the Eindhoven–Leuven–Aachen triangle (ELAT) region of high-tech development (www.solliance.eu).

Alongside these direct-bandgap technologies, IMEC is also researching silicon and organic materials for thin-film solar cells.

CMOS

Aaron Thean, logic program director, presented IMEC's research and aims in the area of logic scaling, including the use of high-mobility channel materials such as indium gallium arsenide (InGaAs, n-channel) and germanium (Ge, p-channel). IMEC has focused in particular on high-mobility-channel integration into CMOS circuity, and boasts record QWFET performance for SiGe (silicon germanium) p-channel transistors (Figure 5).

Thean comments that "band engineering will be required to enhance transport". IMEC's expectation is that such channels will be used at the 10nm node that is being worked on now (2011) with production expected in 2015 (Figure 6).

A variety of institutions around the world are bringing their expertise together to realize such high-mobility channels. However, high mobility is not the only characteristic needed, and some researchers [see, for example, Mike Cooke, Semiconductor Today, vol5, issue 5, p78, June/July 2010] have suggested that III-V channels won't cut it in terms of delivering the needed on/off ratios, sub-threshold swing, drain-induced barrier lowering (DIBL) avoidance, etc.

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Thean comments on these problems: "There are three fundamental classes of challenges that III-V n-channels need to overcome to be a viable high-mobility successor to the Si channel: (1) epitaxy, material defectivity, and integration; (2) transport impact due to density of states (DOS) limitation with the light effective mass; and (3) channel electrostatics and surface passivation that affect DIBL and swing, respectively.

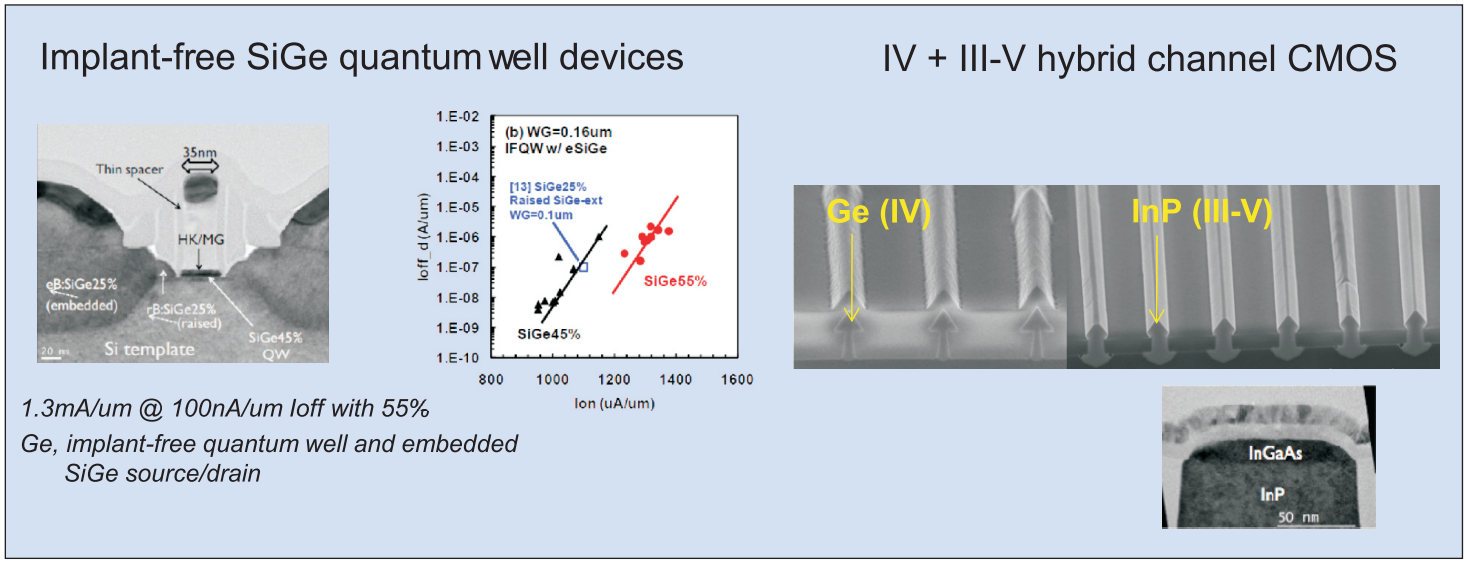

Figure 5. High-mobility-channel devices for 11nm.

"Issues (2) and (3) point to a need to implement new materials with device architectures that can provide improvements in channel electrostatics as well. Fully depleted channel devices like multi-gated FinFETs can lower the channel effective field to mitigate the DOS and DIBL/swing issue. The jury is still out and further investigations are on-going," says Thean.

"Besides the significant work on the material epitaxy and integration, at IMEC much focus is on surface passivation and QW barrier engineering that aligns with the need for further electrostatic improvement. We have gained many insights here and this will help us develop solutions and assess the technology."

On the p-channel side, IMEC has been developing quantum well transistors, starting with silicon germanium. We will continue our path to higher Ge composition, on our way to pure Ge channels: this has helped us understand the process and device issues in a progressive manner

IMEC is also looking at the many alternative possibilities for CMOS channels. "Planar structures are currently being looked at mainly as only a study vehicle, the goal is still to enable a fully depleted channel solution," says Thean. On the p-channel side, IMEC has been developing quantum well transistors, starting with silicon germanium. "We will continue our path to higher Ge composition, on our way to pure Ge channels: this has helped us understand the process and device issues in a progressive manner," adds Thean. ■

The author Mike Cooke is a freelance technology journalist who has worked in the semiconductor and advanced technology sectors since 1997.

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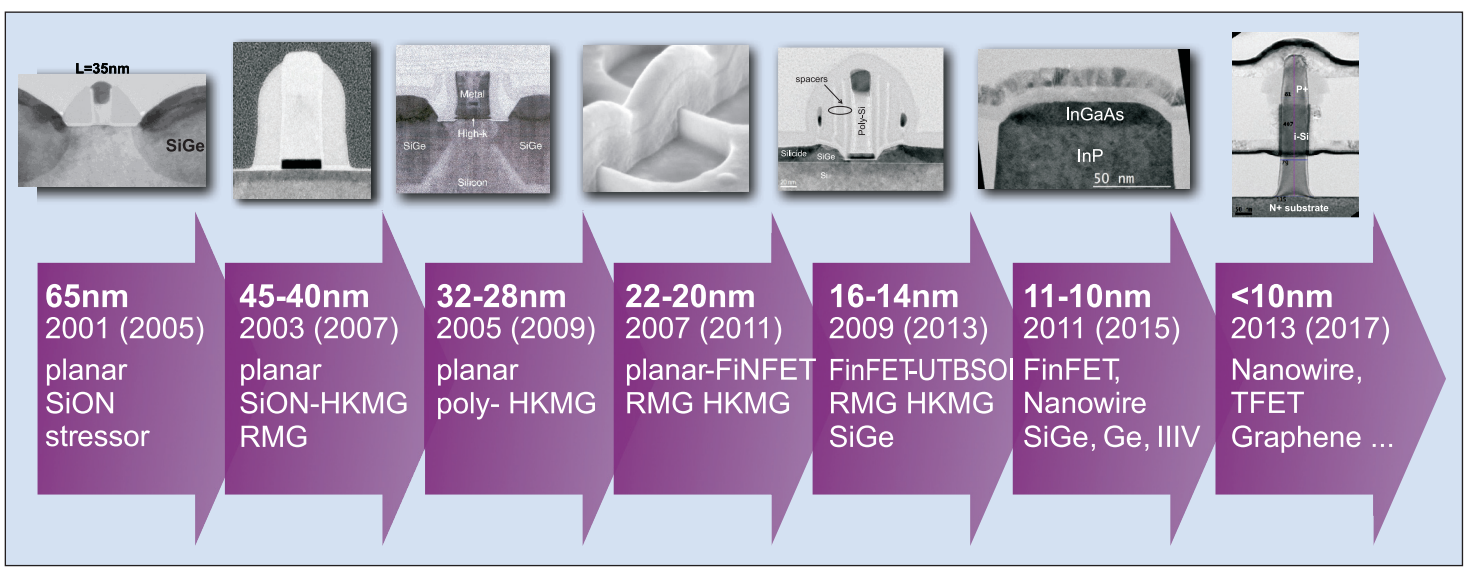

Figure 6. IMEC/ASML roadmap for logic scaling and material innovation.