Developing market for normally-off nitride power electronics

With Japanese companies sampling normally-off gallium nitride transistors, Mike Cooke looks at some recent research towards improved performance.

High-electron-mobility transistors (HEMT) and similar structures based on layers of gallium nitride (GaN) and aluminium gallium nitride (AlGaN) have recently been developed with a view to high-voltage and high-power switching applications. The attractions of these materials include high critical fields and higher switching speeds that allow smaller, more efficient devices to be created. Potential applications cover home appliances, communications and automobiles.

Table 1. Some specifications for transistors sampling from Fujitsu and Panasonic.

	Fujitsu			Panasonic
Parameters	**30V**	**150V**	**600V**	**600V ('tentative')**
Drain current [A]	12	20	20	15
Threshold voltage [V]	1.8	1.8	1.8	1.2
On resistance [mΩ]	12.5	13	92	65
Gate charge [nC]	4	16	12	11
Package (sample)	WLCSP	WLCSP	TO247	TO220

Unfortunately, simple AlGaN/GaN-based HEMTs have a negative threshold voltage, giving a normally-on 'enhancement-mode' operation at 0V gate potential. For safe operation at high voltage or high power densities, transistors with normally-off characteristics are preferred. Further advantages include lower power consumption and simpler drive circuits.

A number of techniques such as fluorine implantation and gate recessing can shift the threshold in a positive direction. However, these methods suffer from thermal stability or process damage problems that impact HEMT performance. Using a metal-insulator-semiconductor (MIS) gate structure can also push HEMT structures into positive threshold voltages.

The Japanese companies Panasonic and Fujitsu even have products for sale (Table 1). These involve processes that grow GaN-based HEMTs on silicon substrates to reduce costs and hence increase market attractiveness.

In March, Panasonic's Industrial Devices Company announced sampling of a GaN-based normally-off power transistor with a blocking voltage of 600V. A few months later in July, Fujitsu released a GaN power device (MB51T008A) with a drain-source breakdown voltage of 150V and normally-off operation — also for sampling — with volume production due in 2014. Other Fujitsu devices with 600V and 30V breakdown characteristics are under development and/or entering sampling aimed at a range of product applications.

Fujitsu sees its 150V-breakdown device as being suitable for high- and low-side switches in DC–DC converters, as deployed in power supplies for data communications equipment, industrial products, and automobiles. The gate structure used to achieve normally-off behavior is described as being 'proprietary'. Company researchers did report in 2010 a MIS-HEMT structure with maximum drain current and threshold voltage of 800mA/mm and +3V, respectively [M Kanamura et al, IEEE Electron Device Letters, vol31, p189, 2010]. The gate was also recessed.

Panasonic's 600V device is produced on 6-inch silicon and uses a p-type gate-injection of holes to achieve normally-off performance. The company claimed that the device was the first to achieve 'failure-free' operation and stable performance in terms of being free from the current collapse effects that are often seen with AlGaN/GaN HEMTs in pulsed operation.

Target applications for Panasonic's device include deployment in power supplies for data-centers/base transceiver stations, and in hybrid electric vehicles (HEV/EV/PHEV).

Despite these 'commercial' products, researchers have not finished work on improving normally-off nitride semiconductor performance. In Europe, the

Framework Programme 7 (FP7) EU project for 'GaN-based normally-off high power switching transistor for efficient power converters' (HIPOSWITCH, www.hiposwitch.eu) involves companies and academic institutes from Austria, Germany, Slovenia, Italy, and Belgium: Aixtron SE, Artesyn Austria GmbH & Co KG, EpiGaN, Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik (FBH), Infineon Technologies Austria AG, Slovak Academy of Sciences, Institute of Electrical Engineering, University of Padua, and Vienna University of Technology. The project was set up in 2011 and is due to finish 2014.

The aim is to produce high-voltage normally-off GaN power devices on silicon substrates with a vertical architecture for technology transfer to a European industrial environment. Since GaN-based devices can theoretically perform reliably at elevated junction temperatures, the team also wants to develop equipment that can handle operation environments up to 225°C.

Thin high-Al content barriers

China's Xidian University has produced 'normally-off' GaN HEMTs with a thin high-Al content AlGaN barrier layer [Kai Zhang et al, Jpn. J. Appl. Phys., vol52, p111001, 2013]. The Xidian approach is similar to gate recessing in that the distance between the gate and channel is reduced. However, gate recessing involves a plasma etch that damages the device structure, leading to higher gate leakage current in operation.

Xidian's nitride semiconductor structure (Figure 1) was grown on c-plane sapphire using metal-organic chemical vapor deposition (MOCVD). A 1.5nm GaN cap layer was applied to the top of the AlGaN barrier. The difference in polarization between the GaN cap and AlGaN barrier created a negative polarization charge at the heterointerface that shifted the threshold voltage in a positive direction. The charge was also expected to enhance the Schottky barrier height of the gate, reducing leakage current.

The ohmic source and drain contacts consisted of annealed titanium/aluminium/nickel/gold. Devices were isolated by plasma etching to a depth of 120nm. Passivation was achieved by plasma-enhanced chemical vapor deposition (PECVD) of silicon nitride (SiN). The passivation reduced the sheet resistance of the two-dimensional electron gas (2DEG) channel by 11% due to a 16% increase in carrier density.

The mobility was slightly reduced by the passivation. It is thought that such passivation mitigates the effects of surface states and defects that can deplete the 2DEG. Possible reasons for reduced mobility include increased electron-electron scattering and/or increased carrier scattering from GaN/AlGaN interface roughness due to the higher carrier density.

The 0.5μm-long gate was formed by creating an opening in the SiN passivation with a plasma etch and depositing nickel/gold/nickel as the gate electrode. Gate and source field plates (FPs) were included in the design to combat current collapse and to push breakdown to higher voltages. The gate FP overhang was 0.3μm (L_{fp1}) and the source FP extension was 0.4μm (L_{fp2}). The gate width was 50μm. The gate–source and gate–drain distances were 0.7μm and 2.6μm, respectively.

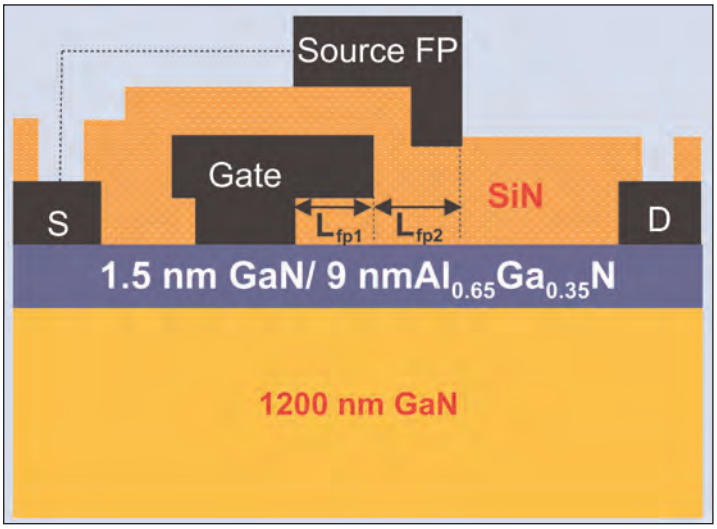

Figure 1. Schematic of fabricated normally-off HEMT with dual field plates. Growth was initiated on the sapphire substrate using a 200nm AlN nucleation layer.

The saturation drain current of the device at 5V drain bias (V_{DS}) and 3V gate potential (V_{GS}) was 441mA/mm. The extrinsic maximum transconductance with the same drain bias was 204mS/mm. The threshold was estimated at +0.3V.

The gate leakage at negative gate potentials was 10^{-7}mA/mm at –5V and 10^{-4}mA/mm at –20V. These low values are attributed to the higher estimated Schottky barrier of 0.91eV compared with barriers in the range 0.5–0.7eV for lower Al-fraction AlGaN (15–35%).

The off-state (–2V gate rather than 0V) breakdown voltage for 1mA/mm leakage was 111V. The gate leakage was significantly lower than the drain leakage. The researchers believe this "suggests enhanced breakdown characteristics can be achieved with further optimization in buffer design, such as lowering the defect density, using compensation iron doping or growing back-barrier layers or double heterojunctions."

The drain-induced barrier lowering (DIBL) was 3.28mV/V over the drain bias range 1–20V. The researchers say that this is "greatly superior" to reported values for AlGaN HEMTs with 25nm barrier and 0.6μm gate length. The improved DIBL is attributed to the high quality of the AlGaN and the use of an insulating buffer layer.

Current-collapse effects were investigated under pulsed operation (Figure 2). An off-state test was used to evaluate gate lag. The researchers comment: "The result indicates that the presented Al-rich AlGaN/GaN

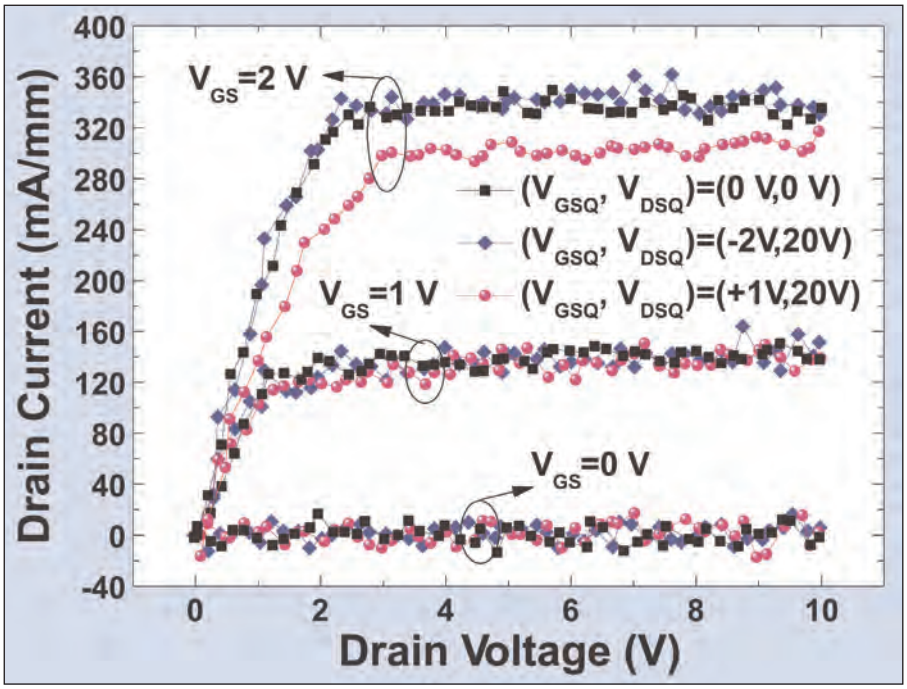

Figure 2. Comparison of pulsed current–voltage characteristics at three quiescent bias points of (V_{GSQ}, V_{DSQ}) = (0V, 0V), (–2V, 20V), and (+1V, 20V), and at V_{GS} = 0, 1, and 2V.

HEMTs do not suffer from gate lag effects induced by surface-related defects at moderate drain bias, originating from the excellent AlGaN quality, Si_3N_4 surface passivation as well as the incorporation of a dual-field-plate design."

The researchers warn that their results were carried out with a relatively low quiescent drain bias of 20V. For power switching applications this should be increased to more than 100V to show the impact of trap charging on dynamic on-resistance.

Current collapse of 12% at 2V gate was seen in the on-state stress testing. "The apparent drain lag effect can be explained as being due to hot-carrier injection into the buffer followed by trapping in deep levels," the researchers write. The team says that more advanced buffer design is needed to tackle this source of current collapse.

The researchers also looked at thermal stability by performing post-gate annealing in the temperature range 200–450°C in steps of 50°C for 10 minutes each. The tests were carried out in nitrogen atmosphere. During the test the threshold voltage was determined. The threshold shifted only 0.045V in the positive direction. The threshold is thus much more stable

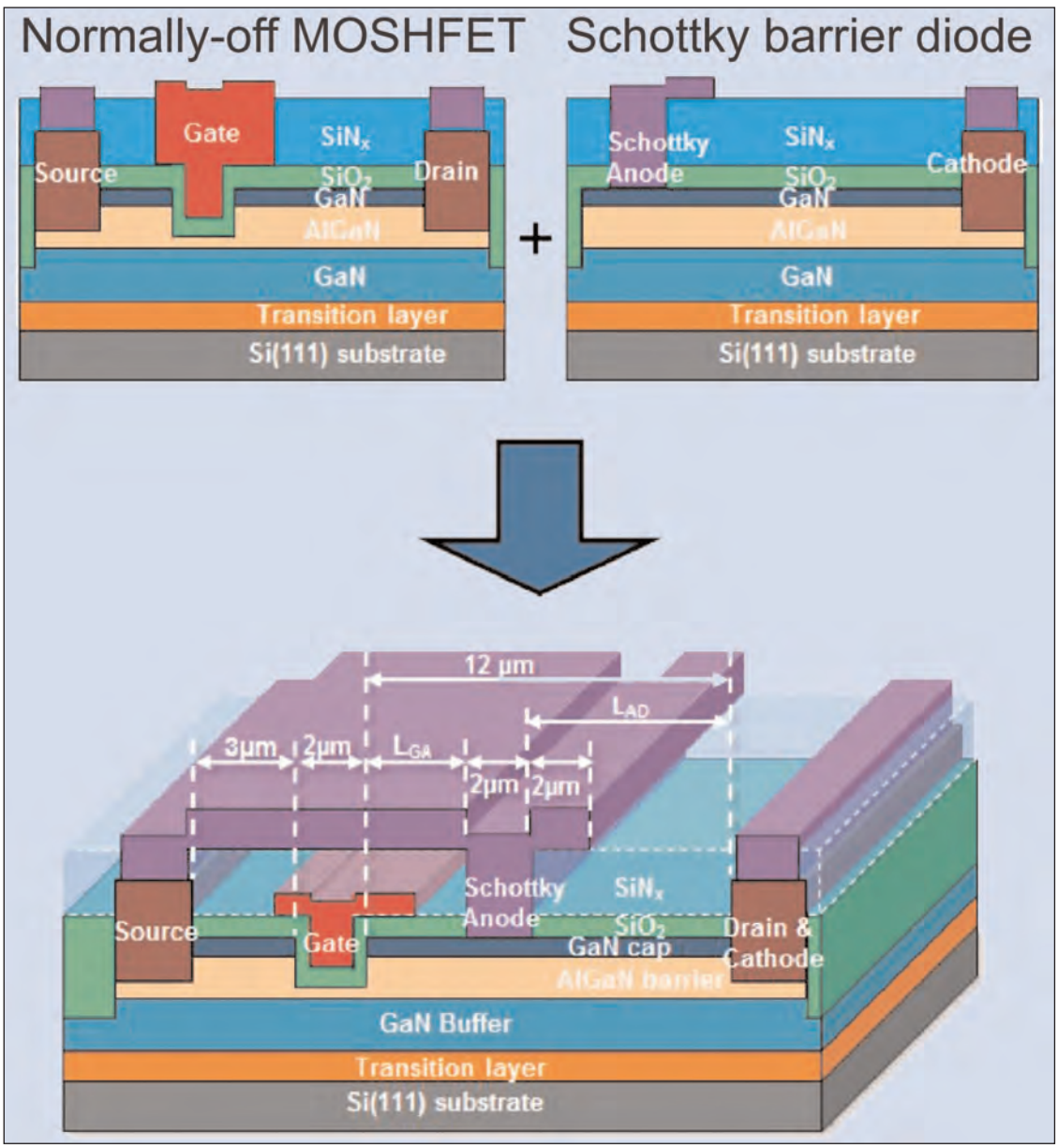

Figure 3. Cross-sectional schematic of SBD embedded AlGaN/GaN-on-Si switching transistor.

compared with fluorine treatments used to give positive-threshold HEMTs, indicating higher reliability for the Xidian devices.

Embedding diodes

A Korea/USA team of engineering researchers has developed a GaN metal-oxide-semiconductor high-electron-mobility transistor (MOSHEMT) with embedded Schottky barrier diode (SBD) [Bong-Ryeol Park et al, Semicond. Sci. Technol., vol28, p125003, 2013]. The researchers were based at Hongik and Cornell universities.

In power switching applications such as for conversion from direct current to alternating current (inverters), circuits often need a Schottky diode, allowing negative current flow during the off-state. If external diodes are used for this, parasitic inductances lead to problems such as ringing, voltage spikes and switching losses.

Some researchers have adopted gate-injection transistor structures (such as those of Panasonic) to avoid the need for external SBDs. These 'GIT' devices have the disadvantage that the rectification and transistor properties are tied together, reducing design flexibility.

Hongik/Cornell adopted a simple method to integrate transistor and diode. The epitaxial undoped AlGaN semiconductor material for the transistor/diode device (Figure 3) consisted of a 4nm GaN cap, 20nm $Al_{0.23}Ga_{0.77}N$ barrier, 1nm AlN spacer, 1.7μm GaN buffer, and AlN/AlGaN/GaN transition layer, grown on n-type (111) silicon.

Mesa isolation was performed with an inductively coupled plasma reactive-ion etch (ICP-RIE). This was followed by gate recess patterning and further ICP-RIE. The recess into the AlGaN barrier had a target AlGaN thickness between the gate foot and GaN buffer of 3nm. The recessing has to be this thin in order for the channel to be completely depleted under the gate, giving the desired normally-off behavior.

Next, a 35nm layer of silicon dioxide was applied using ICP chemical vapor deposition. This layer was then patterned and openings were made for the ohmic contacts with ICP-RIE. The ohmic metals consisted of silicon/titanium/aluminium/molybdenum/gold annealed at 820ºC in nitrogen for 30 seconds. The gate electrode consisted of nickel/gold.

The Schottky barrier diode was created with ICP-CVD of silicon nitride insulation and ICP-RIE/wet buffered oxide etch (BOE) of the anode contact region. The remaining metallization was nickel/gold. The main variable in the devices was the anode-drain distance (L_{AD}) with the related gate-anode distance (L_{GA}) being 10μm — L_{AD}.

The Hongik/Cornell device acts as a normally-off transistor with forward drain bias (Figure 4). The diode blocks current flow. However, with negative drain bias sufficient to turn on the Schottky diode (–1.2V),

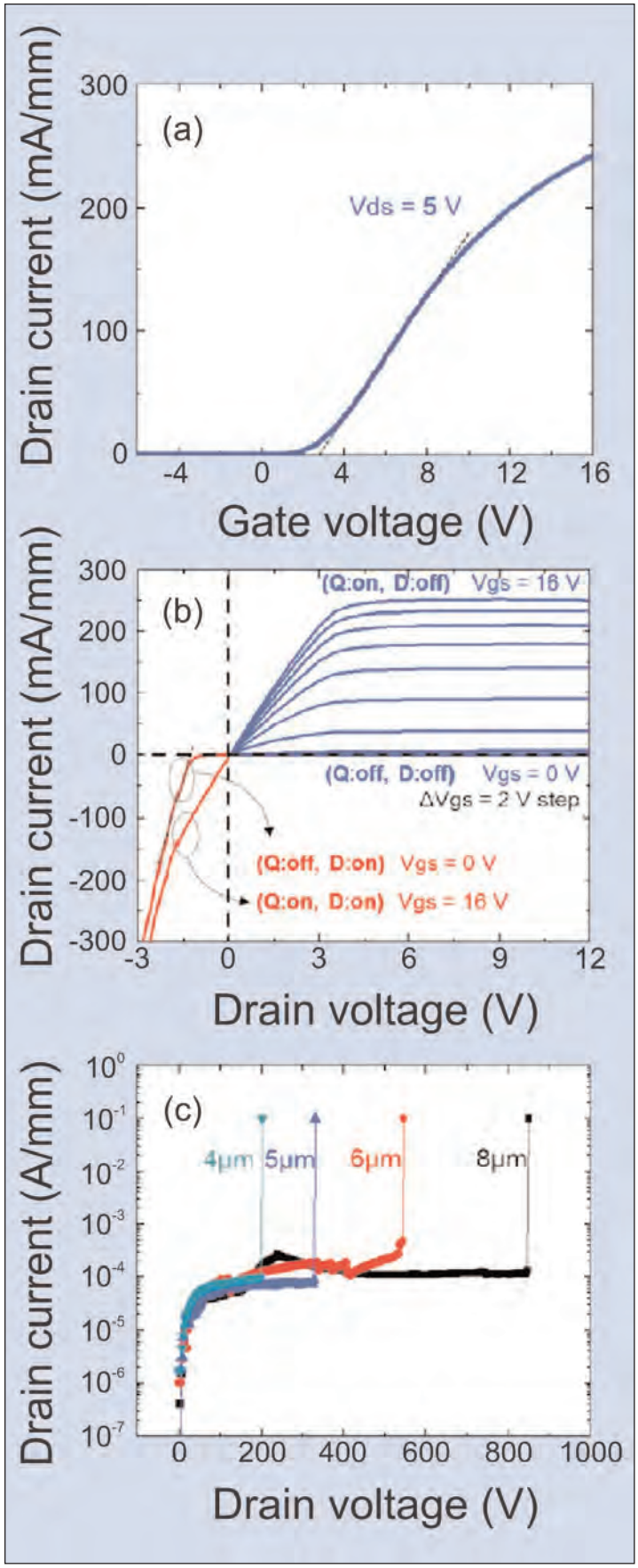

Figure 4. (a) Transfer and (b) drain current–voltage characteristics of the anode-to-drain distance of 8μm and (c) breakdown characteristics of fabricated devices as a function of anode-to-drain distance (L_{AD}).

current flows even when the transistor is off (0V gate) through the anode contact and over through a field-plate structure attached to the source terminal. With the transistor on with a negative drain bias, current flows both through the transistor and the diode structure.

The maximum forward current was 252mA/mm at 16V gate potential. The on-resistance was 2.66Ω-cm^2. The transistor threshold was estimated at +2.8V.

The researchers point out that a significant difference from GIT-type devices is that the Schottky diode turn-on voltage is not affected by the gate potential. This gives an extra degree of freedom for device design. Variations in fabrication such as recess depth and gate dielectric could change the threshold, while the Schottky turn-on could be altered by removing the GaN cap under the anode and/or by changing the metals used.

Off-state breakdown was found for 0V gate as a function of the anode–drain distance. With an L_{AD} of 8\micron, breakdown set in at 849V drain bias. The researchers say that breakdown is governed by the SBD, not the HEMT. Hence, shorter L_{AD} values give lower breakdown voltages.

The researchers speculate that the high leakage current level of ~100μA/mm (0.1mA/mm) in the off state was due to buffer leakage, which could be improved by optimization of buffer quality and better mesa isolation.

The impact of high temperature (up to 300ºC) on device performance was also investigated on devices with L_{AD} of 4μm. The transistor threshold showed no noticeable change. However, the on-currents in both the transistor and diode tend to degrade at elevated temperature. Enhanced thermionic emission also means that the diode turn-on voltage 'decreases' slightly — i.e. it turns on sooner with negative drain bias of the device.

Improving gate swing, avoiding current collapse

Hong Kong University of Science and Technology (HKUST) has developed a 600V GaN-on-silicon (GaN/Si) normally-off metal-insulator-semiconductor high-electron-mobility transistor (MIS-HEMT) with large gate swing and low current collapse [Zhikai Tang et al, IEEE Electron Device Letters, published online 17 September 2013]. The HKUST team raised the threshold voltage of their devices by using fluorine plasma implantation and silicon nitride gate insulator. The MIS-HEMTs also featured a passivation layer that combined aluminium nitride (AlN) and silicon nitride (SiN) to avoid current-collapse effects from charge trapping.

The epitaxial aluminium gallium nitride (AlGaN) structure was grown on 4-inch p-type (111) silicon. The buffer/transition GaN layer was 4μm, on which was added a 1nm AlN spacer, 18nm $Al_{0.25}Ga_{0.75}N$ barrier, and 2nm GaN cap.

Transistor fabrication began with the deposition of ohmic source-drain contacts of thermally annealed titanium/aluminium/nickel/gold. Passivation layers of 4nm AlN then 50nm SiN were added by plasma-enhanced atomic layer deposition (PE-ALD) then PECVD, respectively. Device isolation was achieved using fluorine ion implantation.

Gate formation consisted of making an opening in the passivation layers using a low-power dry etch, treating the gate region with carbon tetrafluoride plasma implantation to shift the threshold voltage to enhancement-mode, the removal of photoresist, ex-situ plasma cleaning in a PE-ALD system to remove surface gallium-oxygen bonds, applying another 17nm of PECVD SiN as gate insulator, and the formation of the nickel/gold gate electrode with 1μm footprint and 0.5μm overhang.

Further dimensions of the tested devices were 1μm gate–source spacing, 10μm gate width and 15μm gate-drain spacing. The resulting MIS-HEMTs were found to have a threshold voltage of +3.6V for normally-off behavior. Comparison HEMT devices with a Schottky gate had a lower threshold of +1.2V. The difference is primarily attributed to "reduced gate-to-channel capacitance by the insertion of the SiN_x gate dielectric" in the MIS-HEMT.

The on/off current ratio was 4x10^9 with a maximum drain current of 430mA/mm. The suppression of gate leakage current enabled by the SiN insulation allowed the device to demonstrate a 14V gate swing. Traditional Schottky-gate GaN HEMTs tend to have the gate swing restricted to less than 3V. The on-resistance for the MIS-HEMT was a 'low' 9.8Ω-mm. The specific on-resistance was estimated at 2.1mΩ-cm^2.

Simple AlGaN/GaN-based high-electron-mobility transistors have a negative threshold voltage, giving a normally-on 'enhancement-mode' operation at 0V gate potential. For safe operation at high voltage or high power densities, transistors with normally-off characteristics are preferred. Further advantages include lower power consumption and simpler drive circuits

Off-state breakdown with a drain current of 1μA/mm occurred at a drain bias of 604V with the gate, source and substrate grounded (0V). Up to 450V, the main leakage comes from the source. At higher biases, gate and vertical substrate leakage increase and become comparable with the source current at 600V. The researchers compared their device with other pub-

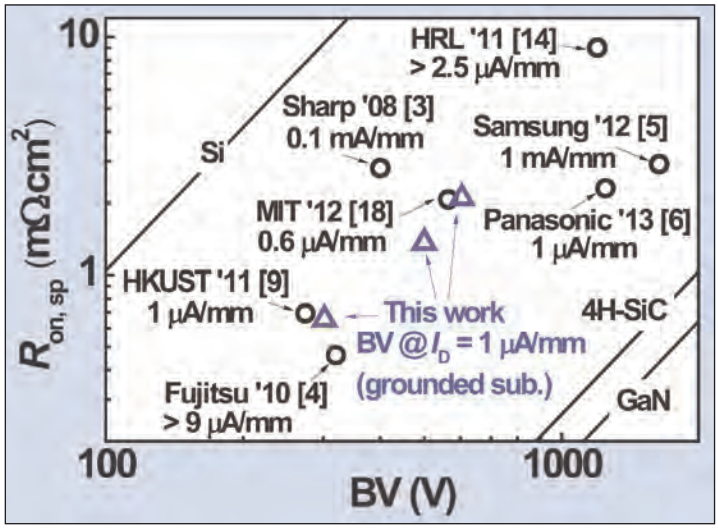

Figure 5. Specific on-resistance (R_{ON}) versus breakdown voltage (BV) of some state-of-the-art GaN-based normally-OFF power devices. OFF-state leakage criteria in defining the OFF-state breakdown voltage in different reports are highlighted.

lished results (Figure 5).

The researchers stress the need for a low off-state current of less than 1μA/mm "to ensure low power dissipation when the device is operated in the high-voltage OFF-state".

The current-collapse effect seen in HEMTs with pulsed bias was assessed using MIS-HEMTs with 1μm gate–source spacing, 2x50μm gate width, 1μm gate length, and 10μm gate-drain spacing. The devices showed "little difference between the dc and pulsed drain current in the linear region" (Figure 6a). Under pulsed operation, self-heating effects are smaller. The researchers suggest this is the reason for the higher drain current in pulsed-mode compared with dc at larger drain bias.

High drain bias stress testing was also carried out (Figure 6b). Below 200V stress, the on-to-off switching time was 0.1 seconds. This increased to 2.7 seconds for higher biases. ■

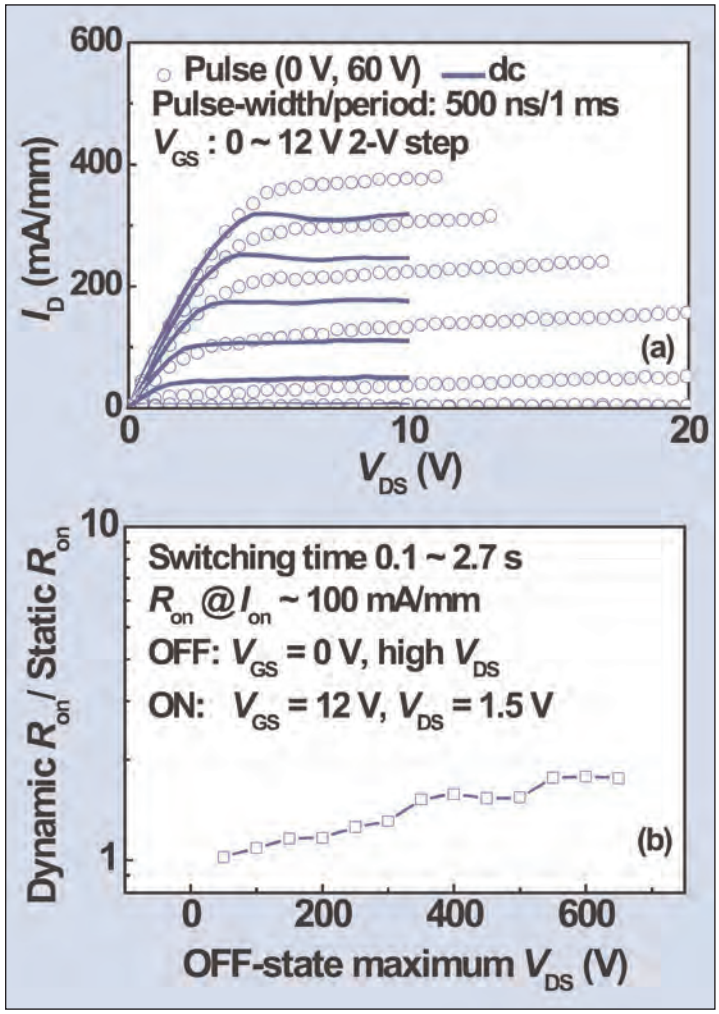

Figure 6. (a) Pulsed drain current versus bias (I_D — V_{DS}) characteristics of E-mode MIS-HEMT with L_{GS} = 1μm, $(W/L)_G$ = 2x50μm / 1μm, and L_{GD} = 10μm. (b) Ratio of dynamic and dc static on-resistance (R_{ON}) obtained by low-speed high-voltage switching measurement on device with L_{GS} = 15μm, $(W/L)_G$ = 10μm / 1μm, and L_{GD} = 15μm.

The author Mike Cooke is a freelance technology journalist who has worked in the semiconductor and advanced technology sectors since 1997.