Re-grown source–drain III-V MOSFETs demonstrate higher drain current

Tokyo Institute of Technology achieves drain current of 1.3mA/μm for InGaAs CMOS field-effect transistors.

The Tokyo Institute of Technology says that it has increased the maximum drain current of indium gallium arsenide (InGaAs) complementary metal–oxide–semiconductor (CMOS) field-effect transistors (FETs) to more than 1.3mA/μm [Ryousuke Terao et al, Appl. Phys. Express, vol4, p054201, 2011].

Researchers have been working to achieve saturation drain currents of 2mA/μm for future scaled CMOS devices and moving from silicon to high-mobility III-V channels such as InGaAs has been developed as an option to achieve this. Earlier this year, a Taiwan National Tsing Hua University/National Taiwan University group reported a drain current of 1.23mA/μm — "to our knowledge, the present maximum drain current", the Tokyo researchers comment.

The Tokyo researchers achieved their improved drain current by increasing the carrier concentration in the source–drain regions through using metal-organic chemical vapor deposition (MOCVD) re-growth rather than ion implantation to create highly silicon-doped InGaAs. The maximum carrier concentrations of ion-implanted InGaAs is about $10^{19}/cm^3$. Using re-growth, this can be increased about 3x.

The epitaxial layers for the latest Tokyo device (Figure 1) were grown on p-type indium phosphide (InP) substrates using MOCVD. The InGaAs channel layer was not doped (intrinsic/i-) to avoid resistance effects arising from ionized impurity scattering. The channel was covered with a thin 5nm i-InP layer to separate the carrier distribution from the oxide interface, avoiding further resistance effects from interface roughness and charge traps. The 300nm i-InAlAs layer below the channel further confined the channel carrier distribution.

A 'dummy gate' structure consisting of silicon dioxide was then formed on the top InP layer with lengths in the range 150nm to 6μm, with a channel width of 20μm. The purpose of the dummy gate was to allow wet etch of the InP and InGaAs layers in the source–drain regions, using hydrochloric acid in water and citric acid in hydrogen peroxide, respectively. The InGaAs etch also undercut the dummy gate on both sides — about 25nm for deep submicron channels (thus 150nm dummy gate gives 100nm channel) and 45nm for micron-scale channels.

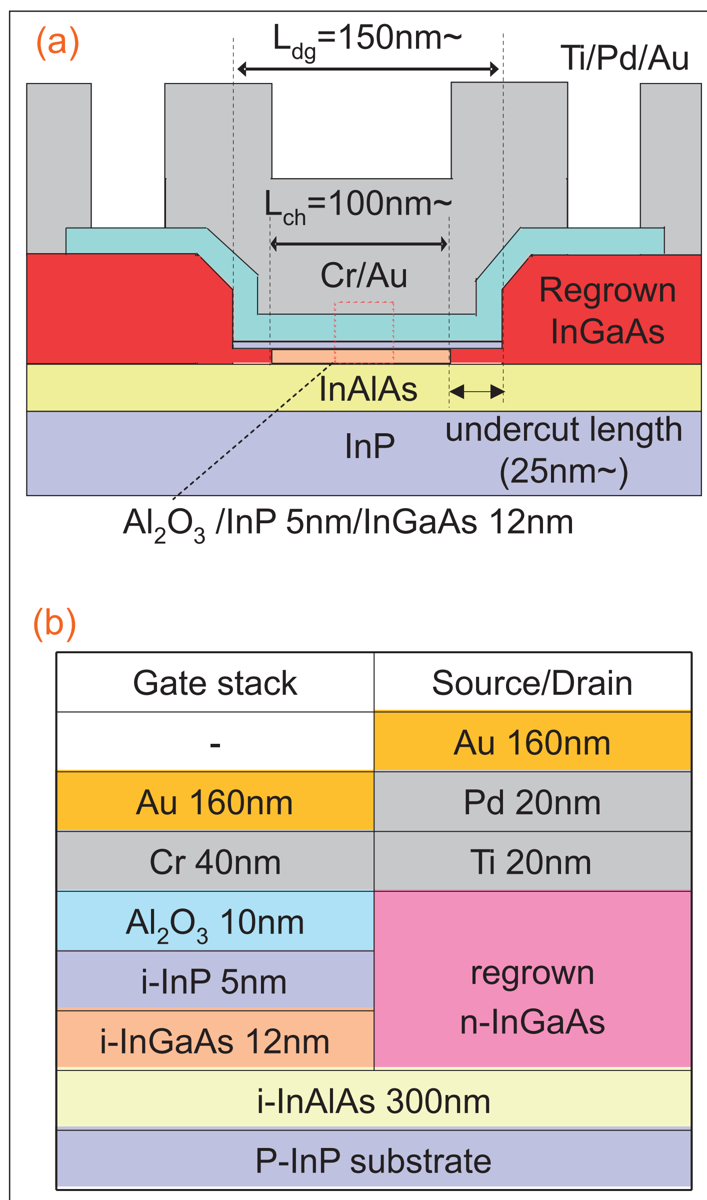

Figure 1. (a) Schematic and (b) layer profile at the gate stack and source/drain structure of the fabricated re-grown source/drain MOSFET.

The wet etch was followed by an InAlAs surface treatment with a more dilute hydrochloric acid solution (1:5 rather than 3:1).

The source–drain regions were then formed from silicon-doped InGaAs regrown using MOCVD. A dummy sample of regrown n-InGaAs on InAlAs/semi-insulating InP was found to have a carrier concentration of $2.9 \times 10^{19}/cm^3$ and a mobility of $1490cm^2/V$-s. "Thus, the re-grown source/drain process seems to be a good technique for heavy doping," comment the researchers.

The devices were then isolated and the dummy gate was removed using buffered hydrofluoric acid. Atomic layer deposition (ALD) was used to apply aluminum oxide (Al_2O_3) gate insulator/dielectric. The wafer was then annealed at 400°C in nitrogen.

The gate electrode metals were then formed and annealed (350°C in nitrogen), followed by etch of the Al_2O_3 and deposition of the source–drain metal.

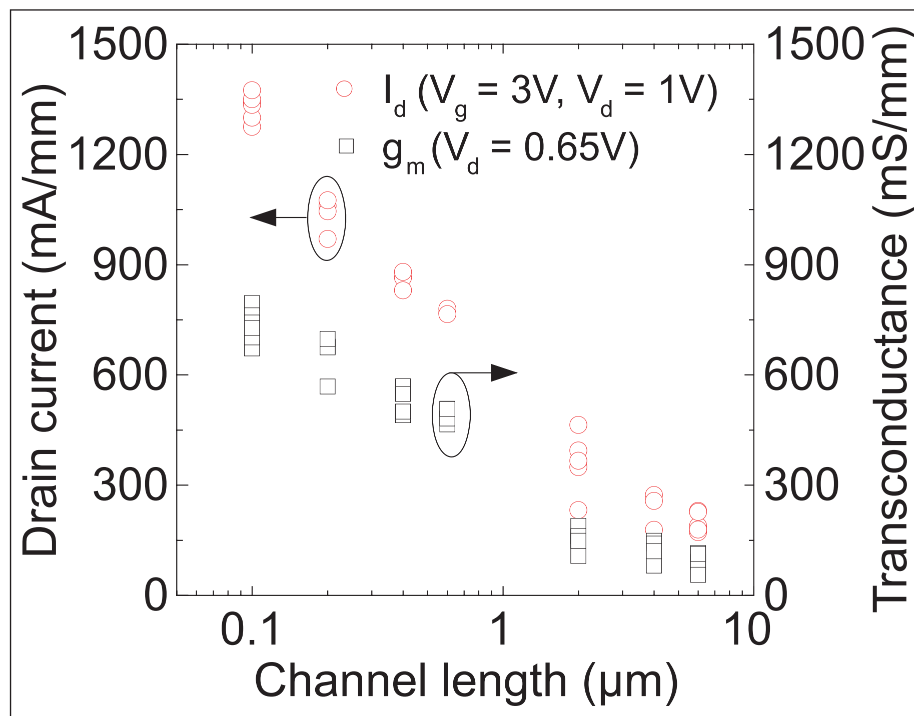

Figure 2. Channel length dependence of drain current (I_d) at drain bias (V_d) 1V and gate potential (V_g) 3V, and peak transconductance (g_m) at V_d 0.65V.

For the shortest channel length of 100nm, the maximum drain current of 1.34mA/µm was obtained with drain bias 1V and gate potential 3V. The gate leakage under these bias conditions was 2.6×10^6mA/µm, a factor of more than 10^5 smaller than the drain current. The peak transconductance of 817µS/µm was obtained at drain bias 0.65V. The threshold was −0.3V, so the device is partially 'on' at 0V (depletion mode, normally-on).

The total series resistance of the MOSFET was 0.5kΩ-µm, "which is slightly worse than other reported values", the researchers comment. The poor series resistance is thought to arise from "high contact resistance of the metal/semiconductor junction". From transmission line method (TLM) measurements, the researchers estimate that 0.38kΩ-µm of the total series resistance arose from contact resistance, with the remainder being due to sheet resistance. Subtracting the series resistance gave an intrinsic transconductance figure of 1330µS/µm. The researchers thus hoped for improved performance from improving the metal/semiconductor contact properties.

One possible reason for the improvement is thought to be a reduction in the dielectric/semiconductor interface trap density as a result of surface cleaning, sulfide treatment, TMA pre-treatments, and annealing before the Al_2O_3 gate dielectric deposition. Comparing the performance of devices with different channel lengths, the researchers note "a good trend of increasing output performance with scaling of the channel length, although we also have room to improve the characteristics by using thinner Al_2O_3"

The estimated peak channel mobility was $3100cm^2/V$-s. The subthreshold swing at a drain voltage of 10mV was 184mV/dec and at 0.65V it was195mV/dec. While these are a way off from the theoretical limit of 60mV/dec of planar MOSFET structures, the researchers comment: "This value is a dramatic improvement compared with our previous device (nearly 1V/decade)". One possible reason for the improvement is thought to be a reduction in the dielectric/semiconductor interface trap density as a result of surface cleaning, sulfide treatment, trimethyl-aluminum (TMA) pre-treatments, and annealing before the Al_2O_3 gate dielectric deposition.

Comparing the performance of devices with different channel lengths (Figure 2), the researchers note "a good trend of increasing output performance with scaling of the channel length, although we also have room to improve the characteristics by using thinner Al_2O_3". There was some degradation of drain current and threshold fluctuation that seem to be associated with charge trapping; further work is needed to analyze and suppress these effects.

The researchers conclude that their results "indicate that the [metal-organic vapor phase epitaxy] MOVPE [i.e. MOCVD] re-growth process has superior capabilities for high-current operation".

http://apex.jsap.jp/link?APEX/4/054201

Author: Mike Cooke