Progress towards combining III-V technology with silicon manufacturing

Mike Cooke reports on contributions to the 'Technology' section of the recent 2014 Symposium on VLSI Technology and Circuits.

Complementary metal-oxide semiconductor (CMOS) transistors based on silicon wafers have been the mainstream of consumer electronics for many decades. As these devices approach atomic limits, new technologies are being sought so that development can continue at the present pace. In the past few years, researchers worldwide have been seeking to combine silicon and III-V electronics — either as a replacement for CMOS or as support for high-frequency functions or optoelectronics.

Silicon provides a low-cost platform for large-scale production, but there are materials with better semiconductor performance. For example, the bulk electron mobility of III-V compound semiconductors such as indium gallium arsenide (InGaAs) can be several times that of silicon ($\sim$1400cm^2/V-s). In electronic devices, the effective mobility is usually significantly less than the bulk value.

Combining the two processing traditions will not be easy. Many of the technologies used for III-V device production are not compatible with those used in silicon semiconductor manufacturing.

Here, we look at some contributions towards overcoming the challenges of combining III-V and silicon technology presented at the recent 2014 Symposium on VLSI Technology and Circuits in Hawaii (9–12 June)

First InGaAs FinFETs on 300mm silicon

A team from the IMEC research center in Belgium reported the first InGaAs Fin field-effect transistors (FinFETs) on 300mm Si substrates [Session 4.1]. Such silicon wafers are presently the largest diameter
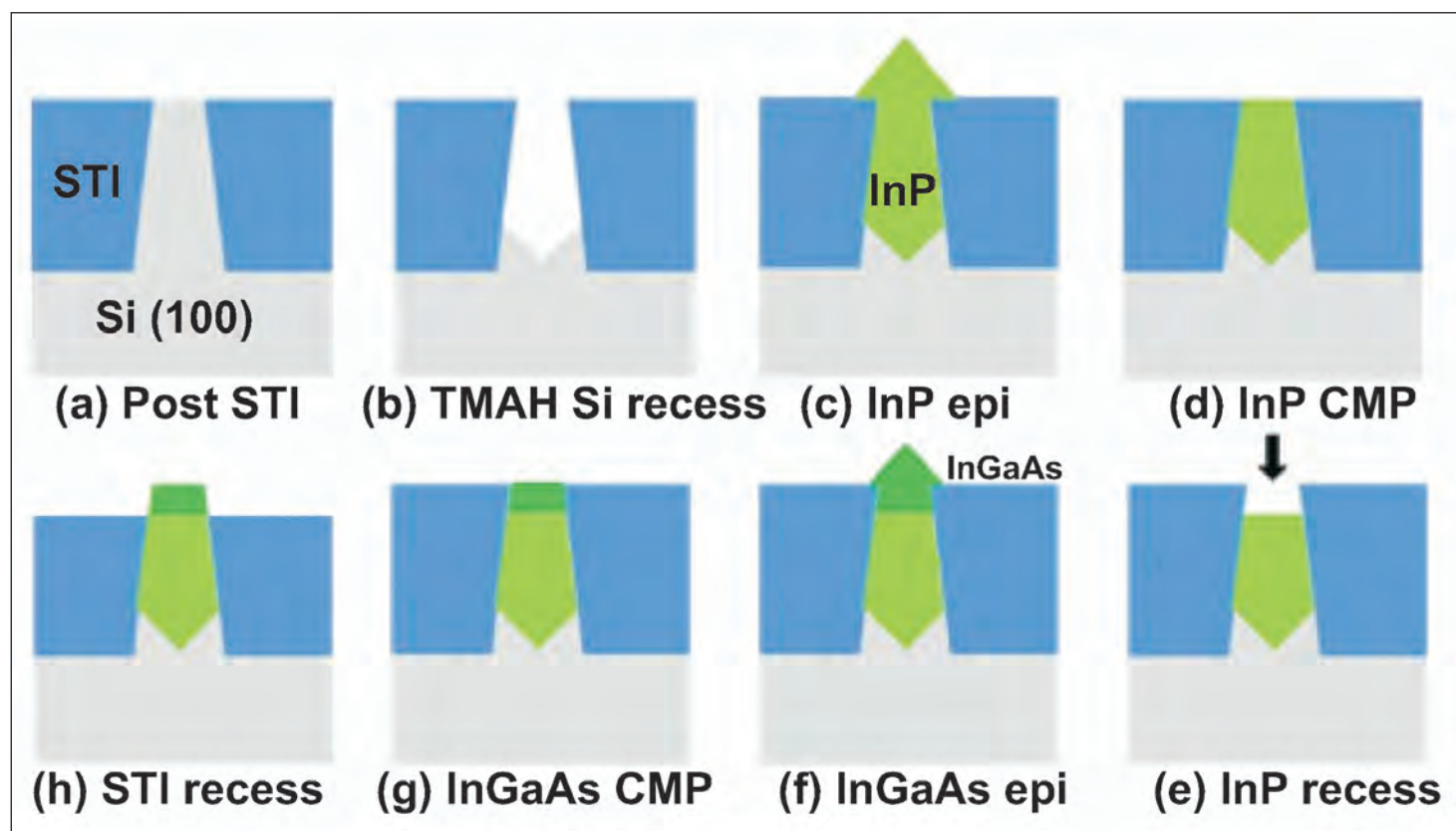

Figure 1. Process flow for IMEC's InGaAs fin formation on 300mm Si (100) substrates.

commercially available and form the basis for mass electronics manufacturing.

The researchers used a shallow trench isolation template as the basis for creating the InGaAs fins (Figure 1). Such templates consist of shallow trenches filled with dielectric/oxide insulator between silicon fins. The silicon fins were etched out and replaced with indium phosphide (InP) through metal-organic chemical vapor phase epitaxy (MOCVPE). The excess InP was removed with chemical mechanical planarization.

The InP material was further recessed to form the base of the InGaAs fin with target In content of 53% for lattice matching with InP. The InGaAs was doped with magnesium to provide p-type conductivity, overcoming the donor effect of carbon from the metal-organic deposition process. The magnesium doping was needed to avoid buffer leakage, but could not be too high or mobility degradation would result.

After another round of CMP, the fin was revealed with a SiCoNi selective etch of the STI oxide. SiCoNi is an Applied Materials etch process that provides 20:1 selectivity for silicon dioxide (SiO_2) over silicon. SiCoNi is marketed mainly as a 'pre-clean' for cobalt/nickel physical vapor deposition.

Raised source/drain (S/D) regions consisting of silicon-doped n-InAs were grown around dummy gates. A 'high-k last' replacement metal gate (RMG) process was used with a stack consisting of 2nm aluminium oxide (Al_2O_3), 3nm hafnium dioxide (HfO_2), 3nm titanium nitride and tungsten plug contact on titanium liner. The high-k last process avoids thermal degradation during the high-temperature (more than 500°C) InAs S/D deposition. The equivalent oxide thickness (EOT) of the stack was 1.9nm.

A 50nm-gate-length transistor with optimized buffer/channel doping achieved a subthreshold swing (SS) of 190mV/dec and an extrinsic peak transconductance of 558µS/µm. The researchers comment: "Optimization of the devices for best short-channel and on-state performance will require a more detailed study of the process window for InP and InGaAs Mg doping next to a more aggressive EOT and fin width."

The IMEC team has also been developing InGaAs quantum well (QW) metal-oxide field-effect transistors (MOSFETs) [Session 19.1]. The QWMOSFETs (Figure 2) were grown on indium phosphide substrates. The quantum well structure was grown first up to a 20nm heavily doped n-InGaAs cap layer. The InGaAs cap layer provided protection of the underlying layers during high temperature S/D re-growth.

The device fabrication began with electron-beam lithography in hydrogen silsesquioxane (HSQ) to provide a mask for the S/D metal-organic chemical vapor
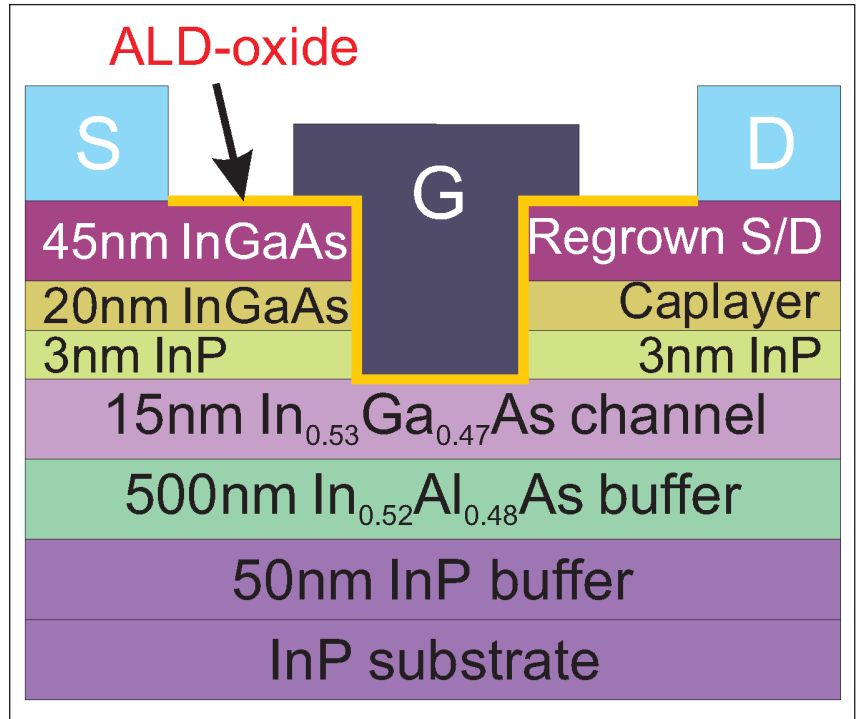

Figure 2. Device with nominal layer thickness.

deposition (MOCVD) re-growth. The S/D regions consisted of $In_{0.53}Ga_{0.47}As$ doped to a concentration of $2\times10^{19}/cm^3$.

After forming an isolation mesa, the InGaAs cap and InP layers were removed. A 3-cycle digital etch (atomic layer deposition in reverse) was performed to give a clean InGaAs channel surface on which to deposit the gate dielectric.

Three different gate dielectric recipes were studied: 5nm Al_2O_3, 2nm/3nm Al_2O_3/HfO_2, and 1nm/3nm Al_2O_3/HfO_2. These resulted in equivalent oxide thicknesses (EOTs) of 2.5nm, 1.6nm, 1.1nm, respectively. The gate electrode was aluminium. The completed devices were subjected to annealing in forming gas (H_2/N_2).

Initial tests on the three device types suggested that even the very thin EOT of 1.1nm was sufficient to block gate leakage current and that there was room for further EOT thinning.

A 75nm gate length device with 1.1nm EOT demonstrated an on-current of 470µA/µm at 0.5V drain bias, an off-current of 100nA/µm, and peak extrinsic transconductance of 2.35mS/µm. The SS was 87mV/decade at 0.5V drain and 84mV/decade at 0.05V. The threshold voltage was slightly negative at –0.1V.

The team comments: "Our devices exhibit highest I_{on} and $g_{m,ext}$ among InGaAs-channel MOSFETs at a large L_g range, approaching InAs devices. Meanwhile, SS remains the lowest for planar III-V MOSFETs. These advances emerge from the high-quality dielectric/III-V interface, S/D re-growth, and epitaxy, especially the very low background doping in InAlAs buffer which gives low I_{off} and better electrostatics." ►
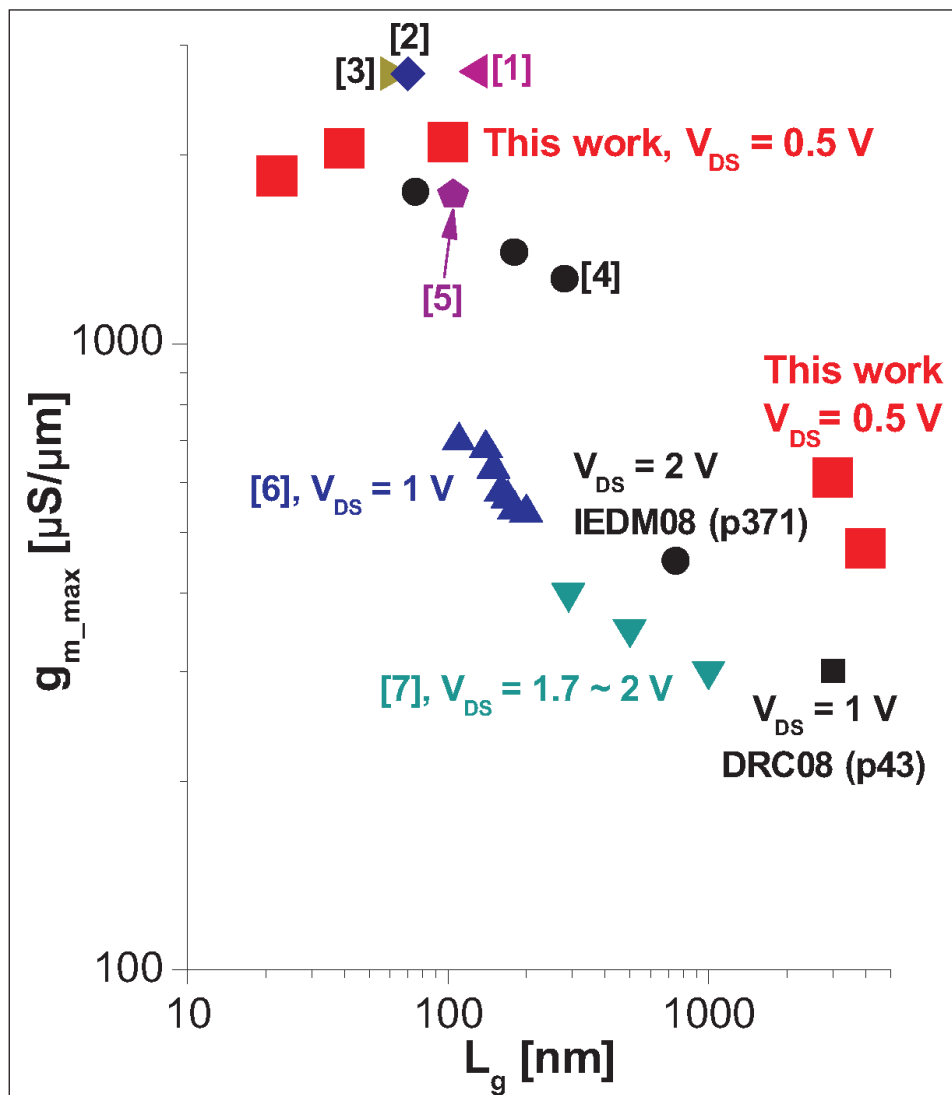
Figure 3. Peak transconductance ($g_{m.max}$) versus gate length for Pennsylvania/Samsung InGaAs QW MOSFETs with re-grown S/D by MOCVD ("this work"), as well as other reports. Long-channel devices exhibit record $g_{m.max}$ behavior.

▶ Pennsylvania State University and Samsung Electronics reported on joint research into the effect of varying the indium content of InGaAs in QW FinFETs (QWFFs) [Session 8.4].

The researchers used heterostructure materials grown using molecular beam epitaxy (MBE). First, a gate recess region was created with a citric acid wet etch selective to indium phosphide. This step cut through the cap layer and produced raised S/D regions. The fins were created with 100nm pitch using electron-beam lithography and chlorine-based plasma etch. The high-k gate dielectric consisted of 1nm/3nm atomic layer deposition (ALD) Al_2O_3/HfO_2. Palladium was used as gate electrode. The S/D ohmic contacts were titanium/gold.

The researchers found that the highest on-current was obtained with $In_{0.7}Ga_{0.3}As$ quantum well fin channels of 38nm width. A 1µm gate-length device had a peak mobility of 3000cm^2/V-s, compared with

1450cm^2/V-s for an $In_{0.53}Ga_{0.47}As$ channel. A non quantum well finFET with $In_{0.53}Ga_{0.47}As$ channel had a mobility of 1000cm^2/V-s.

A short-channel QWFF with gate length 120nm and fin width 55nm achieved a saturation drain current of 1.16mA/µm with the gate at 1V over threshold. The extrinsic peak transconductance was 1.9mS/µm at 0.5V drain bias. The off-current was 30nA/µm. The SS was 236mV/decade.

QW-MOSFET records

Korea Advanced Nano-fab Center (KANC), Yonsei University, SEMATECH and GLOBALFOUNDRIES reported on a gate-last (GL) process for InGaAs QWMOSFETs with record performance [Session 4.3].

The researchers attribute their results to the gate-last process with "selective S/D regrowth by MOCVD to improve scalability and contact resistivity, optimized gate stack process with thin EOT and low [interface trap density] D_{it} to improve SS, and gate-last process to maintain excellent carrier transport of the InGaAs channel."

The device material was grown on InP substrates using MBE. The undoped 10nm $In_{0.7}Ga_{0.3}As$ channel layer was deposited on $In_{0.52}Al_{0.48}As$ back-barrier. The S/D contacts were grown around an HSQ dummy gate.

The transistor fabrication involved mesa isolation, molybdenum S/D contacts, and atomic layer deposition of Al_2O_3/HfO_2 gate dielectric and titanium nitride gate electrode.

Long-gate (5µm) devices with equivalent oxide thickness of 1nm demonstrated SS of 80mV/decade and drain-induced barrier lowering (DIBL) of 22mV/V. The effective mobility was greater than 5500cm^2/V-s.

The researchers comment: "The mobility in this work is one of the highest reported for any surface-channel MOSFET, with EOT close to 1nm. This is a record for a III-V MOSFET, arising from both the optimized GL integration flow and low-D_{it} gate stack process with Al_2O_3/HfO_2 that benefit fully from the high electron mobility associated with the $In_{0.7}Ga_{0.3}As$ channel."

On the basis of the high effective mobility, the device also exhibited record transconductance for longer gate lengths (Figure 3).

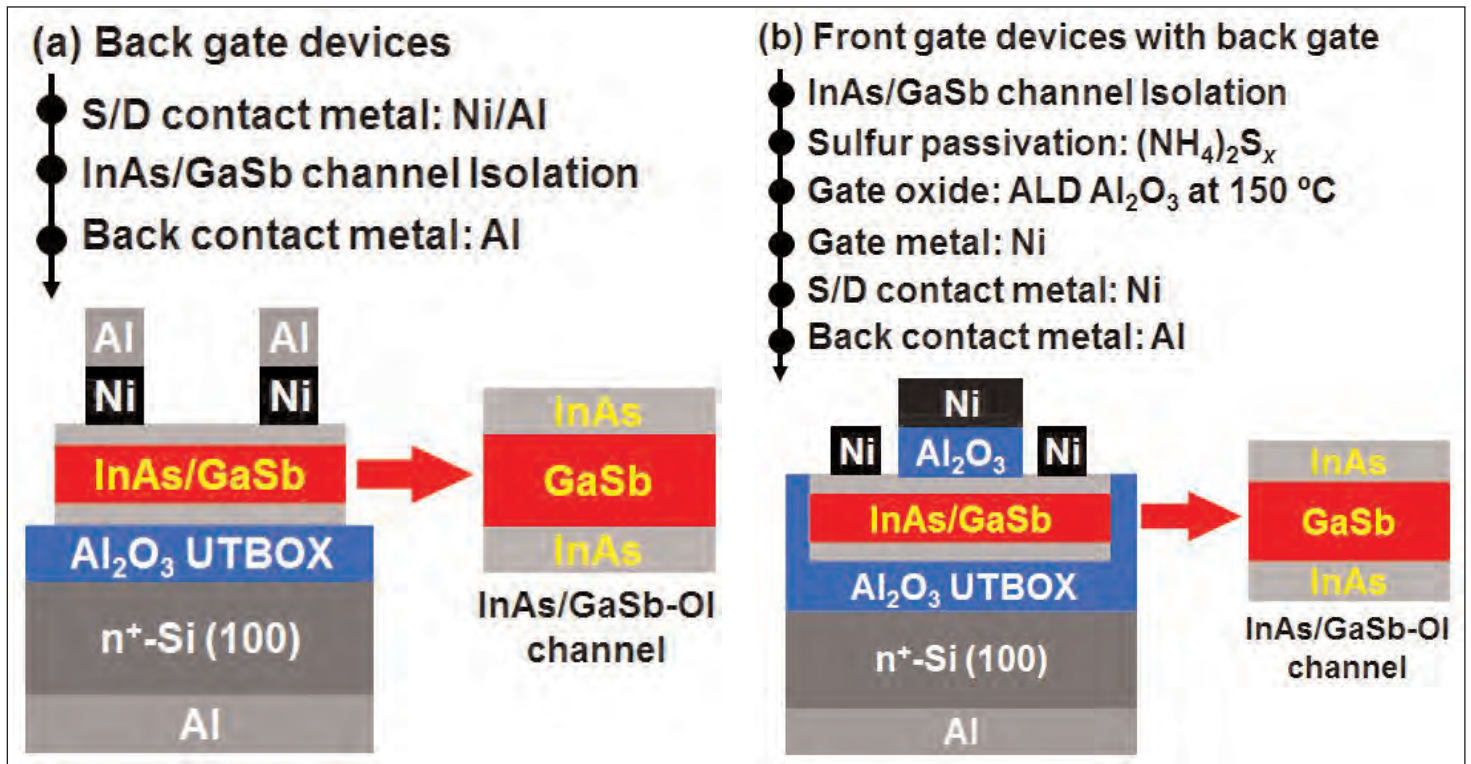A short-gate (40nm) transistor had a somewhat higher SS of 105mV/decade and DIBL of 150mV/V.

Figure 4. Fabrication process flow of (a) back-gate devices and (b) front-gate devices with back gate.

At 0.5V drain bias, the peak transconductance was "fairly high" at 2mS/μm. Going to even shorter gates of 22nm, the SS more than doubled to 250mV/decade (DIBL 450mV/V). The researchers see this as indicating the need for '3D channel architectures' — in other words, finFETs and the like.

The team believes improved short-channel performance can be achieved through development of a self-aligned process for the S/D contacts.

Single-structure InAs/GaSb CMOS

University of Tokyo, NTT Corporation, and the Japanese JST/CREST funding program have developed a single structure of indium arsenide and gallium antimonide (InAs/GaSb) that can be used to create both n- and p-MOSFETs [Session 4.2]. The aim of the work is to avoid the problems of combining III-V n-type devices with germanium p-type transistors with different structures for complementary metal-oxide semiconductor (CMOS) performance. The researchers believe an all-III-V CMOS solution would be easier to integrate.

The heterostructure consisted of GaSb sandwiched between ultrathin layers of InAs grown on InAs substrate. Simulations suggested that the structure could support both n- and p-type channels where the charge carriers are electrons or holes, respectively. The structure was transferred to silicon through direct wafer bonding. The adhesion was between layers of aluminium oxide on both the III-V heterostructure and the silicon wafer.

Transistors were fabricated in two different configurations (Figure 4). In one type, the electrostatic control was though a simple back gate with an aluminium back contact through the silicon wafer. A more sophisticated transistor consisted of both front- and back-gate contacts.

With just the back gate, the researchers demonstrated both n- and p-MOSFET performance. Hole mobility with an InAs thickness of 2.5nm and GaSb thickness of 20nm was better than silicon-based devices. With 5nm InAs and 20nm GaSb, the electron mobility was 1200cm^2/V-s – again better than bulk silicon. The electron mobility decreased with thinner 2.5nm InAs, but the value was still greater than obtained for ultrathin silicon-on-insulator devices. "These results indicate that III-V channels can maintain an advantage against Si channels even with the ultrathin-body CMOS structures," the researchers say.

The more sophisticated devices allowed the threshold voltage of the front gate to be controlled by the back gate. When the back gate potential was –2V, pMOSFET behavior was observed in devices with 2.5nm InAs and 20nm GaSb. Setting the back gate to –0.5V gave nMOSFET performance in the same devices.

University of Tokyo and JST/CREST have also worked with US company IntelliEPI Inc to develop a direct wafer bonding (DWB) process that could transfer III-V layers to larger-diameter silicon wafers [Session 4.4]. The researchers reported: "We have demonstrated InGaAs-OI MOSFETs on Si by using the InGaAs channels on Si donor wafers, for the first time."

Usually, DWB transfers layers from much smaller wafers of III-V substrates such as InP. These wafers are often limited to diameters of about 2 inches, while
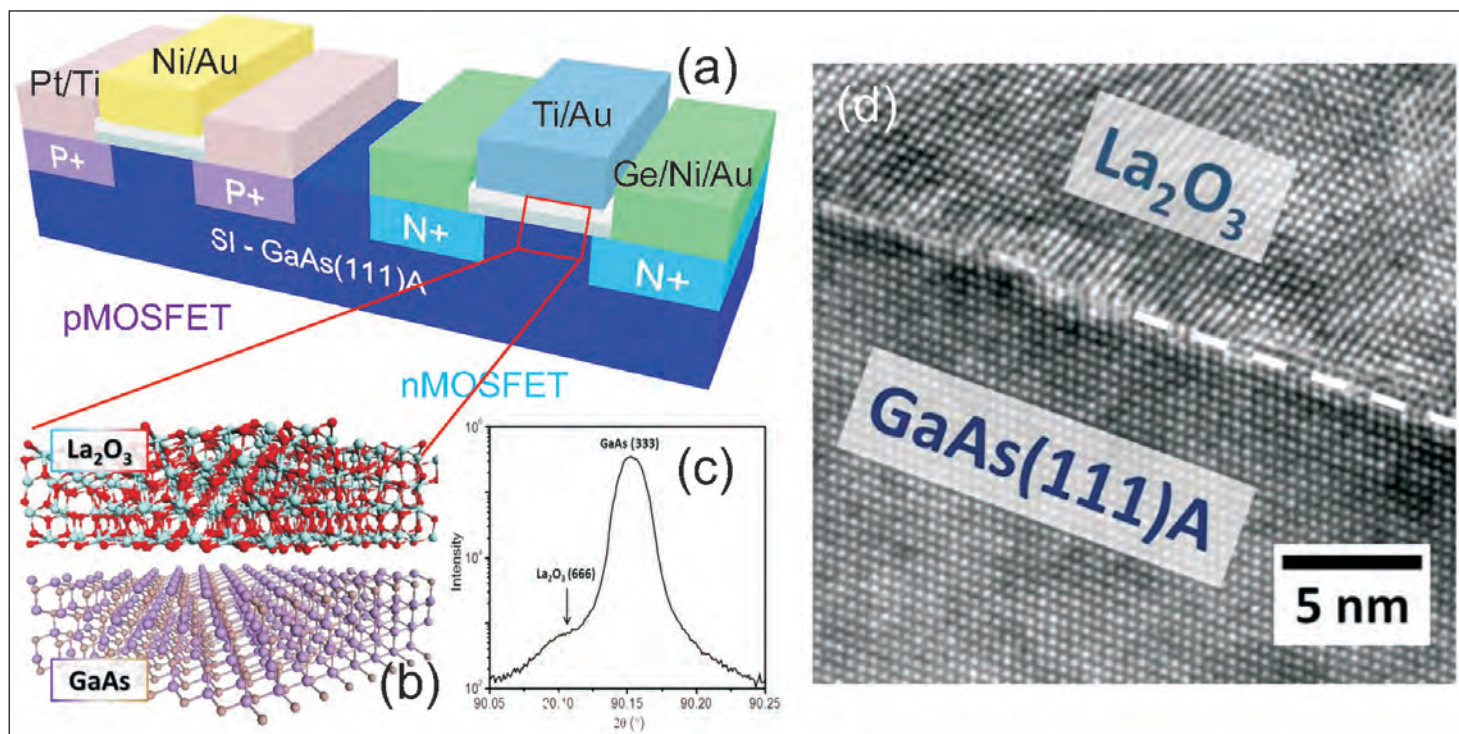
Figure 5. (a) Schematics of GaAs pMOSFET and nMOSFET. (b) Atomic structure view of single-crystalline La$_2$O$_3$ layer over GaAs(111)A surface. (c) High-resolution x-ray omega-two theta coupled scan for La$_2$O$_3$ on GaAs (111)A. (d) HR-TEM image of a La$_2$O$_3$/GaAs(111)A epitaxial interface.

mass-production silicon manufacturing prefers larger 300mm (12-inch) diameter wafers. In the future, large-scale manufacturers plan to implement 450mm diameters.

Instead of using III-V donor wafers to create the heterostructures, a silicon donor wafer was prepared by growing InAlAs/GaAs buffer layers and the InGaAs channel using MBE. The InGaAs channel layer was found to have mobility 6550cm^2/V-s and carrier con-

centration 1.5x10^{17}/cm^3 at 300K.

The direct wafer bonding was prepared by depositing Al$_2$O$_3$ on both the donor and target wafer surfaces, followed by CMP. A further layer of HfO$_2$ was deposited on the wafers before bonding. The donor wafer silicon handle and buffer layers were removed by etching with tetramethylammonium hydroxide (silicon), citric acid (GaAs), and hydrochloric acid (InAlAs).

The result was "very uniform formation of a high-
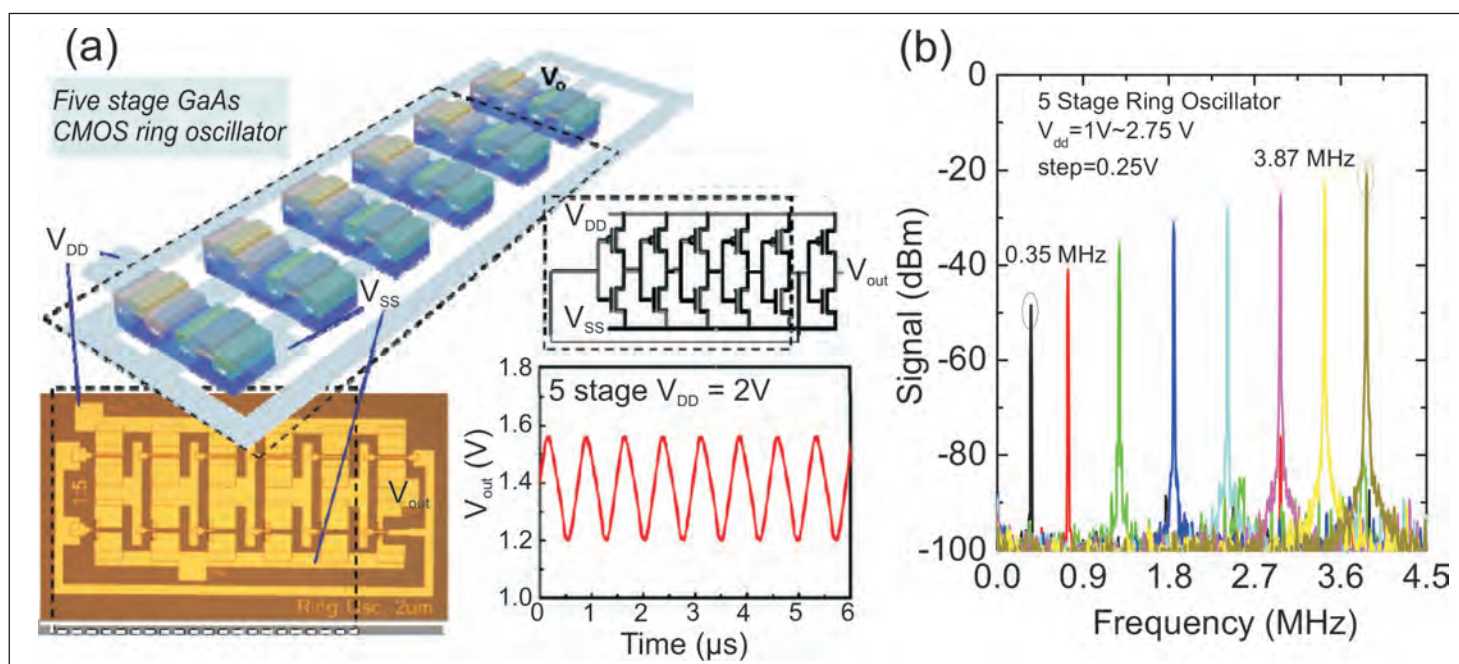

Figure 6. (a) Illustration, circuit schematic, optical micrograph and output characteristics of a GaAs CMOS five-stage ring oscillator. (b) Measured output power spectrum of five-stage GaAs CMOS ring oscillator.

quality 10nm-thick InGaAs-OI wafer on a Si substrate, transferred from a Si donor wafer," according to the researchers. Performance of the InGaAs material was similar to that of InGaAs grown on III-V substrates in terms of photoluminescence and Raman spectroscopy. The root-mean-square surface roughness was 1.4nm, according to atomic force microscopy.

The material was used to create MOSFETs with 10nm Al_2O_3 gate dielectric and tantalum gate metal. The S/D contacts were nickel. With a channel thickness of 9nm and gate length of 1µm, the SS of the MOSFETs was 100mV/decade and the on/off-current ratio was more than 10^6. The effective electron mobility was 1700cm^2/V-s – a three-fold enhancement over silicon-based devices, according to the researchers.

GaAs CMOS

Purdue and Harvard universities jointly claimed the first high-performance GaAs CMOS devices and circuits [Session 6.4]. The researchers used complementary metal-oxide semiconductor (CMOS) field-effect transistors (FETs) created with a lanthanum oxide (La_2O_3) dielectric (Figure 5). The circuits included inverters, NAND and NOR logic gates, and five-stage ring oscillators.

The La_2O_3 dielectric layers of the devices were fabricated with atomic layer epitaxy (ALE). A capping layer of Al_2O_3 was added to protect the La_2O_3 from the air. X-ray analysis suggested that the lattice mismatch between the La_2O_3 and underlying GaAs(111)A material was only 0.04%.

A 1µm-gate-length nMOSFET had a maximum drain current of 376mA/mm at 2V drain bias and 3.5V gate potential. The SS was 74mV/decade. The equivalent oxide thickness was 3nm. The peak effective electron mobility was 1150cm^2/V-s.

Similar pMOSFETs achieved maximum drain currents of 30mA/mm (800°C) and SS of 270mV/decade (780°C). Unfortunately, there is a trade-off in annealing temperature between drain current and SS. Higher temperatures lead to higher drain current but also poorer SS and low on/off-current ratio. The peak effective hole mobility for 780°C annealing was 180cm^2/V-s.

An inverter circuit based on these components achieved a gain of 12 at 3V operating voltage. The NAND/NOR logic gates achieved output voltages of 0V/2.5V with 0V/2.5V inputs. The ring oscillator (Figure 6) frequencies at 1V and 2.75V were 0.35MHz and 3.87MHz, respectively. ■

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