Upwardly mobile III-V- and Ge-based transistors

Researchers from around the world reported progress in enhancing transistor performance through semiconductor material engineering at the 2012 IEEE Symposium on VLSI Technology in Hawaii. Mike Cooke reports.

Prospects of radical changes in mainstream semiconductor device technology in the coming years have attracted specialists in III-V semiconductors, along with those promoting the wider use of germanium. Here we look at the contributions in these directions at June's 2012 IEEE Symposium on VLSI Technology in Honolulu, Hawaii.

Scaling III-V transistors

The University of Tokyo, Japan's National Institute of Advanced Industrial Science and Technology (AIST) and Sumitomo Chemical reported the first demonstration of sub-60nm deeply scaled indium gallium arsenide (InGaAs)- and indium arsenide (InAs)-on-insulator (OI) metal-oxide semiconductor field effect transistors (MOSFETs) on silicon (Si) substrates [S. H. Kim et al, session 21.1].

Often InGaAs devices are grown on indium phosphide (InP) substrates, but for mass production these devices need to be produced on Si. The base III-V-OI structures used by Kim et al were formed by the transfer of layers grown on InP to a silicon dioxide layer on silicon.

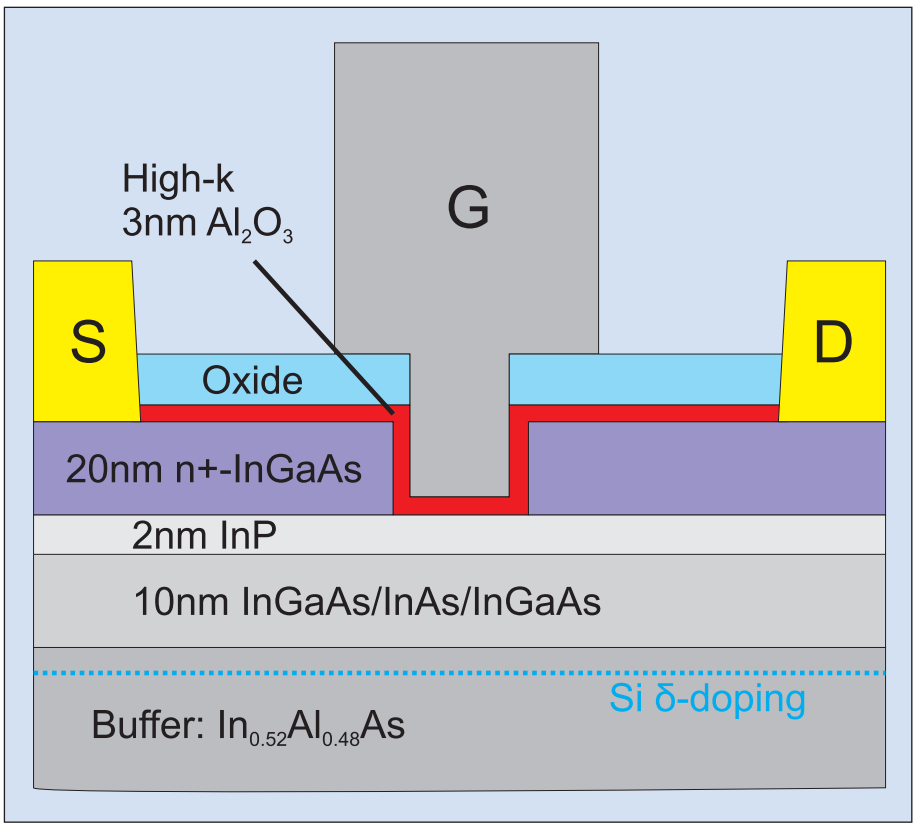

Figure 1. Schematic cross-section of quantum well device created by SEMATECH, University of Modena & Emilia, CNSE, Teledyne and MIT.

Then devices were created using MOS interface buffer engineering and nickel-InGaAs source–drain regions to achieve a 400% increase in on-current over an InGaAs control device with the same drain-induced barrier lowering (DIBL) of 100mV/V and an off-current of 1nA/μm.

An InAs–OI device with a 55nm channel gave a small DIBL of 84mV/V and a subthreshold swing (SS) of 105mV/dec. The use of InAs allowed the researchers previously to create MOSFETs with high mobility performance values up to 3180cm^2/Vs.

SEMATECH, University of Modena & Emilia, CNSE, Teledyne, and MIT also used InAs, this time to produce quantum well devices (Figure 1) with record transconductance of 1.73mS/μm, and record high frequency cut-off (f_T) and maximum oscillation (f_{max}) values of 245GHz and 355GHz, respectively [T.-W. Kim et al, 21.2]. The gate length was 100nm. The researchers used an aluminium oxide/indium phosphide (Al_2O_3/InP) gate stack to give a low density of interface traps that can degrade transistor performance. The researchers see III-V channels as especially promising for low-power logic applications.

Pennsylvania State University and the US Naval Research Lab used antimonide (InAsSb) quantum wells to achieve a record mobility of 6000cm^2/V-s in a long-channel (20μm gate) device [A. Ali et al, 21.3]. The high-k dielectric gate insulator consisted of 1nm of Al_2O_3 and 10nm of HfO_2. A short-gate (150nm) transistor

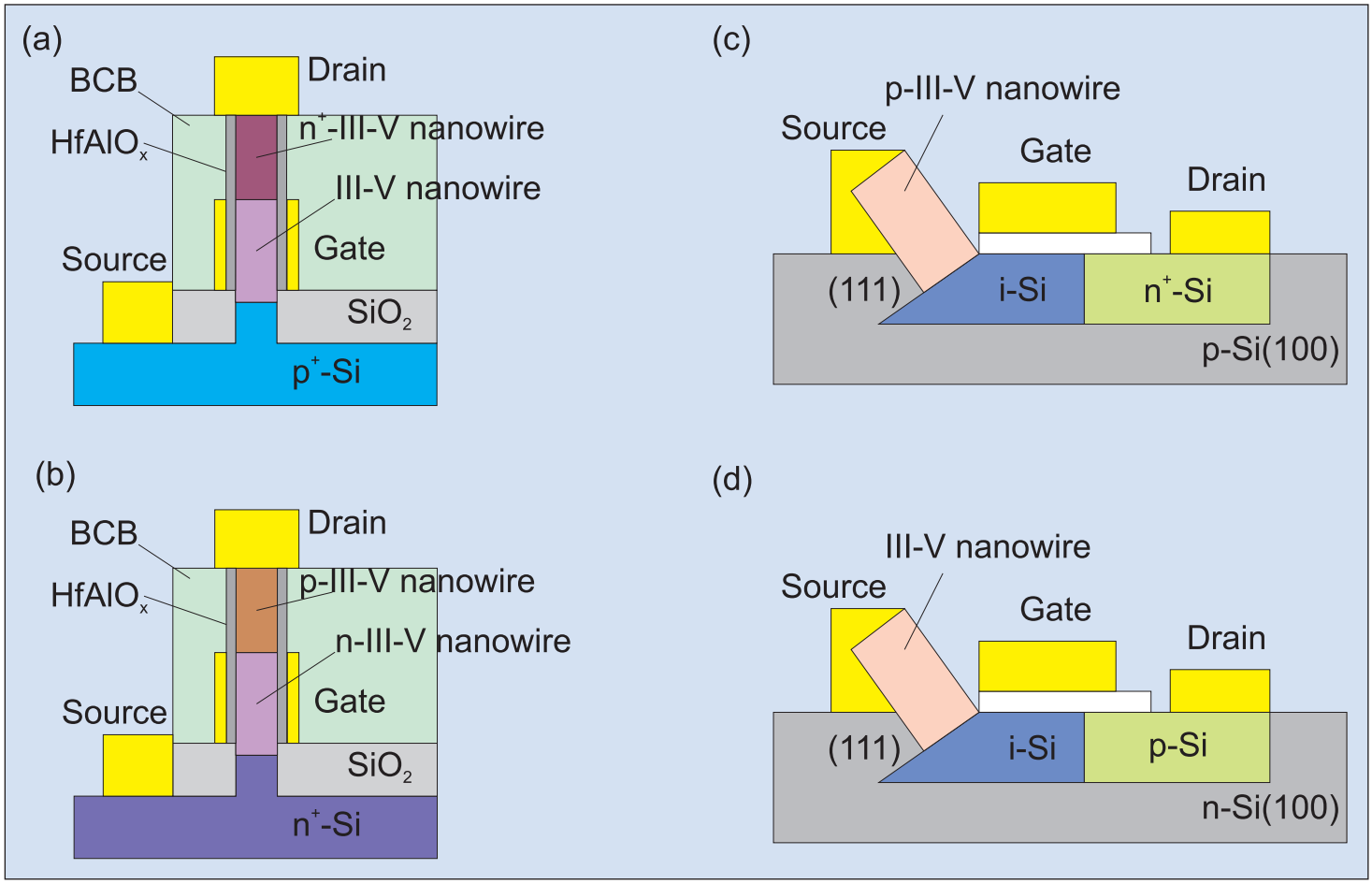

Figure 2. Schematics of Hokkaido University/JST TFETs using III-V NWs/Si heterojunctions. (a), (b) vertical surrounding-gate type TFETs on Si(111) surfaces using Si as source and III-V NWs as gate and drain region. (c), (d) planar type TFET on Si(100).

achieved an f_T of 120GHz. The 120GHz cut-off and (cut-off x gate-length) product value of 18GHz-μm are claimed to be "the highest for any III-V MOSFET" (presumably before the presentation of SEMATECH et al with f_T x L_G of 24.5GHz-μm). The Pennsylvania State University/Naval Research Lab devices were depletion-mode/normally-on, but the researchers reported that the preferred enhancement-mode/normally-off performance had recently been demonstrated.

Stanford University, Applied Materials and US Naval Research Lab reported some preliminary theoretical and experimental explorations of InGaSb as a high-mobility channel material for both NMOS and PMOS, giving complementary MOS (CMOS) behavior, as used in mainstream integrated circuits [Z. Yuan et al, 21.5].

Electron and hole mobilities in excess of 4000cm^2/V-s and 900cm^2/V-s, respectively, can be achieved using InGaSb. Although performance of transistors was restricted by contact and series resistance effects, the researchers comment: "This is, to our best knowledge, the first demonstration of a high-mobility NMOS and PMOS in the same channel material with comparable I_{ON}, thereby making InGaSb an attractive channel material for realizing complementary logic in III-Vs."

Low power, steep subthreshold

Hokkaido University and Japan Science and Technology Agency (JST) – PRESTO presented InAs nanowire (NW) tunneling field-effect transistors (TFET) with subthreshold swings as low as 21mV/dec [Katsuhiro Tomioka et al, 6.3]. The formation process was similar to that reported by the same group at IEDM 2011 [Mike Cooke, Semiconductor Today, February 2012, p93], with InAs replacing InGaAs.

The nanowires consisted of vertical NWs of InAs material grown on p-Si (111) using metal-organic vapor phase epitaxy. The transistors were constructed with the deposition of a hafnium dioxide/aluminium oxide/tungsten (HfO_2/Al_2O_3/W) gate stack and etch-back to define a gate length of 200nm (Figure 2a,b). The source was given by a titanium/gold back-contact on the p-Si wafer. The drain was given by titanium/aluminium/titanium/gold deposited on the exposed tips of the NWs.

Although the initial devices had a high SS of 104mV/dec, this was improved by enlarging the drain region (decreasing contact resistance) and reducing the NW diameter (increasing heterojunction resistance and lowering defect densities). By reducing the NW diameter from 90nm to 30nm, the SS at 1V drain bias

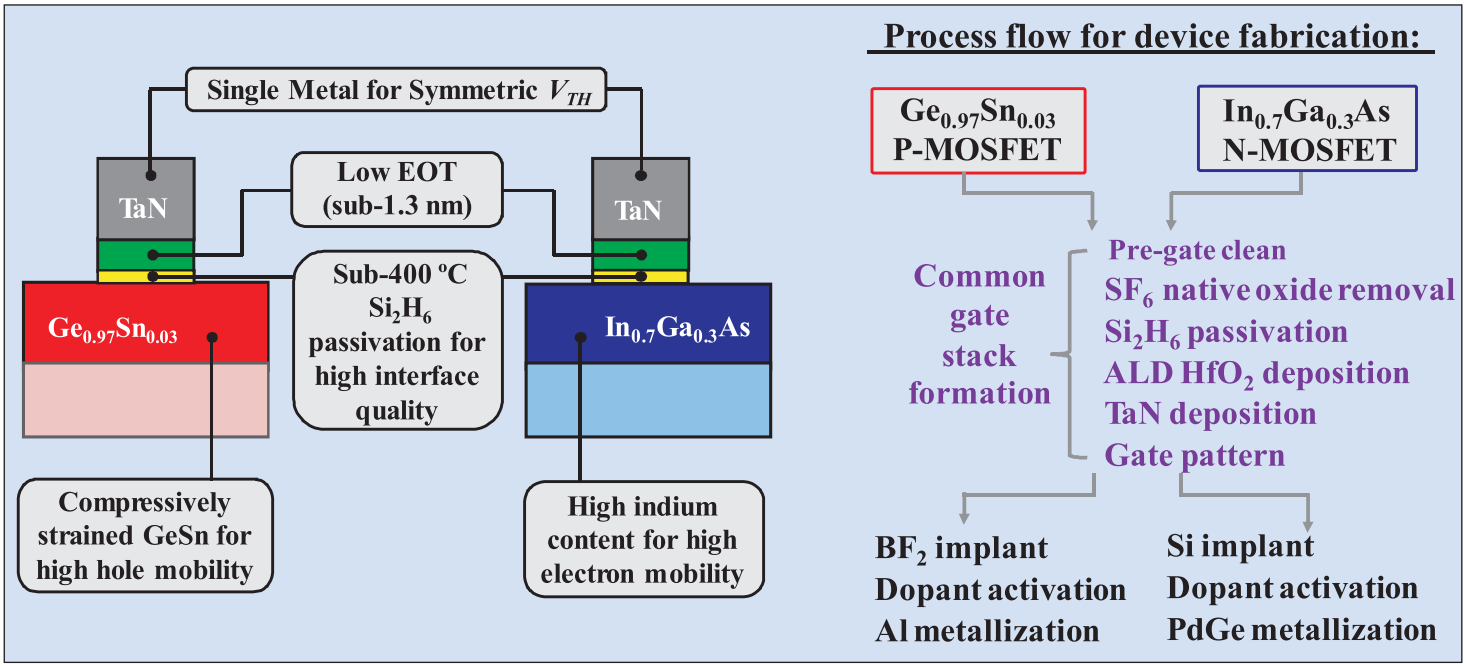

Figure 3. Left, key highlights of Singapore/China common gate stack technology for $Ge_{0.97}Sn_{0.03}$ P-MOSFET and $In_{0.7}Ga_{0.3}As$ NMOSFET. Right, process flow with Si_2H_6 passivation technique developed to achieve high interface quality, transport carrier confinement, and reduced gate leakage current.

was reduced to as low as 21mV/dec (average 25mV/dec). This beats the ~60mV/dec theoretical limit of planar CMOS at room temperature. The on–off ratio of the NWTFET best device was 10^6.

The devices were grown on Si (111) crystal orientation rather than the Si (100) used in CMOS production. However, the researchers suggest that they could be incorporated into the mainstream by angled growth (Figures 1c, d).

Intel Corporation reviewed its III-V MOSFET and TFET research [G. Dewey et al, 6.2]. The company sees III-V devices, "especially the 3D tri-gate MOSFET and TFET" as viable options for future ultra-low-power applications. Intel also reported simulations of expected improvements from the use of TFET architectures [Uygar E. Avci et al, 21.4]. Disappointing performance in experiments on large devices was suggested as being due to geometrical factors. The modelers comment "Results suggest the III-V TFET with optimized electrostatics is a realistic candidate to outperform CMOS at low supply voltages to improve logic energy efficiency."

Mobility enhancements

National University of Singapore reported the first demonstration of germanium telluride as a liner stressor for FinFETs [Ran Cheng et al, 11.1]. The material was converted from an amorphous to crystalline material in a thermal anneal step at 220ºC, resulting in a 10% volume contraction, thus setting up compressive stress in the silicon channel. The stress increased the mobility of the channel so that the maximum drain current was increased by 69% in a device with a 30nm liner stressor (33nm before anneal) and 106% in one with a 50nm liner stressor (55nm pre-anneal), at a fixed off-current of 10nA/μm. The researchers also claimed that the 3nm gate length of their devices was the shortest reported to that date.

A relatively new mobility enhancement is from the use of germanium tin (GeSn) semiconductor layers. Although GeSn is normally proposed for pMOS, Stanford University, IMEC, KULeuven, and GLOBALFOUNDRIES reported the first experimental realization of GeSn nMOSFETs [S. Gupta et al, 11.2]. The researchers grew GeSn (5% Sn) layers using atmospheric-pressure chemical vapor deposition. NMOS transistors were formed gate-last with phosphorous-doped source drain regions. The gate oxide was Al_2O_3. Devices with and without a 5nm Ge cap were produced.

The devices were found to have poor activation of the implanted P doping, even after thermal annealing, giving large source–drain parasitic resistance. Further problems include significant interface trap densities and compressive strain in the channel. These factors limit device performance compared with theoretical simulations suggesting better electrical behavior over pure Ge NMOSFETs. The Ge cap is found to offer some improvement and the researchers comment: "Further enhancements in GeSn nMOSFETs can be obtained by employing implant-free S/D technology, [and] strain engineering to introduce channel tensile strain."

National University of Singapore, Chinese Academy of Sciences' State Key Laboratory on Integrated Optoelectronics, and Singapore's Institute of Materials Research and Engineering also report "the world's first

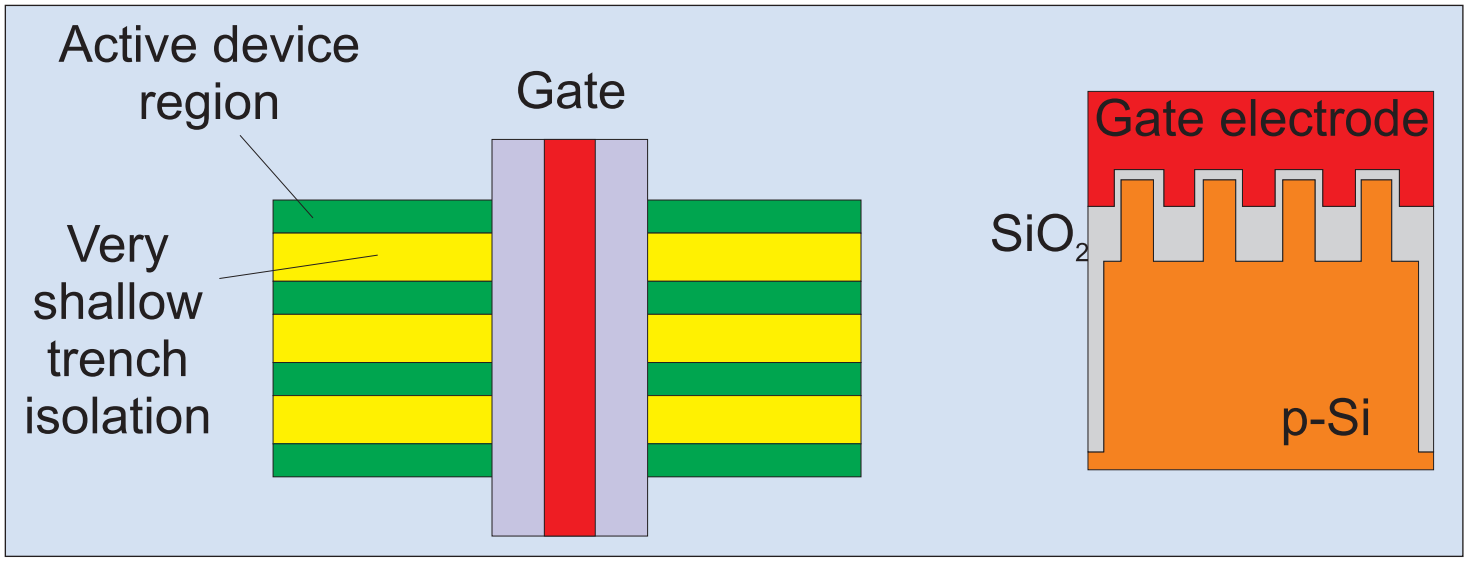

Figure 4. Plan view (left) and cross-sectional view (right) across the gate of UCB/Applied Materials/Soitec SegFET structure.

germanium-tin (GeSn) channel nMOSFETs" [Genquan Han et al, 11.3]. The 170nm p-GeSn channel was grown on Ge using molecular beam epitaxy (MBE). The Sn composition was 2.4%. The gate-last process used a native oxide ($GeSnO_2$) interlayer between the channel and the high-k gate dielectric of tantalum nitride/aluminum oxide. The SS was 128mV/dec. The on–off ratio was ~10^4.

The Singapore/China researchers also presented a common gate stack for high-performance GeSn PMOS and InGaAs NMOS, giving a potential CMOS solution [Xiao Gong et al, 11.4]. The equivalent oxide thickness of the HfO_2 gate dielectric was less than 1.3nm (Figure 3). The gate metal was tantalum nitride. The passivation was provided by silicon delivered through disilane (Si_2H_6) applied at relatively low temperatures of less than 400ºC.

The researchers report: "Using this gate stack, the world's first GeSn short-channel device with gate length (L_G) down to 250nm was realized. Drive current of more than 1000μA/μm was achieved, with peak intrinsic transconductance of ~465μS/μm at V_{DS} of −1.1V."

The team was keen to find ways to implement a common surface passivation and gate stack, since such processes are preferred in manufacturing because of the reduced number of process steps. The channel materials with 3% Sn and higher-than-usual indium content (70%) were designed to boost mobility performance for holes and electrons, respectively.

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The 250nm short-channel GeSn device had even higher Sn content of 5%, along with other factors used to improve the performance of such components: S/D extension (SDE), halo implant, spacer formation and deep S/D implant, etc. The researchers believe that lower source/drain resistance combined with shorter gates will lead to improved saturation drain current performance.

Ge-based devices

For pure Ge PMOS transistors, University of Tokyo reported record high hole mobility of 596cm^2/V-s with 0.8nm equivalent oxide thickness [R. Zhang et al, 19.1]. The gate stack consisted of $HfO_2/Al_2O_3/GeO_x$/Ge. University of Tokyo has developed a plasma post-oxidation (PPO) method using an electron cyclotron resonance oxygen plasma. Previously the researchers have used the method to create aluminium oxide, but with a view to thinner equivalent oxide thickness (EOT), they have now applied it to hafnium dioxide, with aluminium oxide used as a diffusion control layer, giving better MOS interface control.

Japan's AIST and Meiji University have created Ge nanowire pMOSFETs with records for high inversion hole mobility of 855cm^2/V-s and for saturation drain current at 1V bias of 731μA/μm [Keiji Ikeda et al, 19.3]. The NWs were subjected to compressive strains of up to 3.8%. Metal source/drain regions were used. Both the channel and source/drain regions were undoped, avoiding process variability arising from impurity fluctuations. The gate length for the record device was 65nm. The Ge channel was formed by a two-step condensation of SiGe-on-insulator.

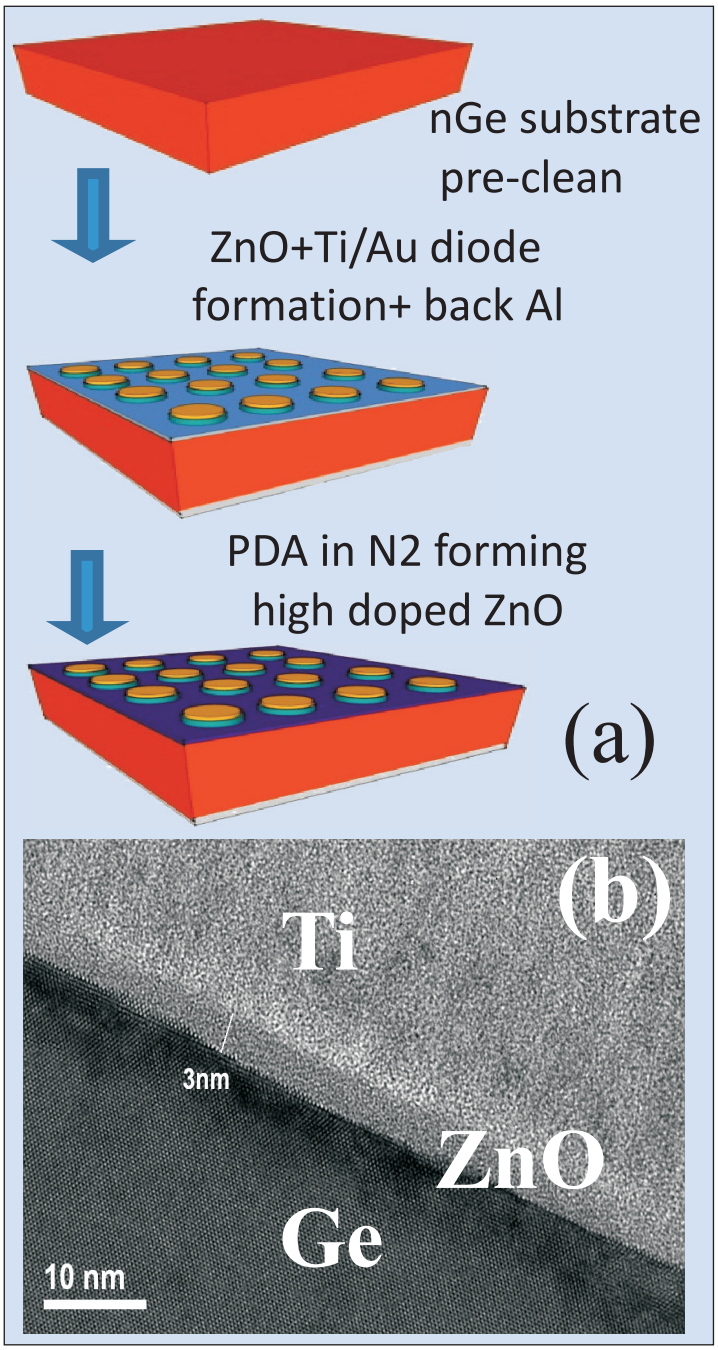

Figure 5. (a) Indian Institute of Technology Bombay/ Applied Materials process flow for making ohmic contacts on n-Ge using ZnO. (b) TEM of Ti/ZnO/Ge interface.

University of California at Berkeley, Applied Materials, and Soitec reported 30% improved on-current for SiGe channel pMOSFETs with segmented channels over planar SiGe channels [Byron Ho et al, 19.4]. Over pure Si reference devices, the on-current was increased by 70%. The off-current was 10nA/μm layout width. The 70nm-wide Si/SiGe/Si (20nm/3nm/3nm) stripes were grown in gaps between 30nm-wide SiO_2 lines (Figure 4).

IMEC has been developing SiGe implant-free quantum well (IFQW) structures for PMOS [J. Mitard et al, 19.2]. Studies suggest that the key parameter for improving performance is mobility improvement, rather than gate-length reduction.

ZnO in advanced Si, Ge, SiC transistors

Finally, and slightly to one side, Indian Institute of Technology Bombay and Applied Materials have made simulations and experiments of the use of n-type zinc oxide as an interfacial layer between metal and n-type semiconductor [P. Paramahans et al, 9.4]. Among their aims is to create lower-resistance ohmic source–drain contacts than the present silicide (metal-silicon compound) technology.

In particular, complications in using silicides arise as the devices are scaled to smaller dimension. Further, higher-mobility transistors using germanium channels suffer from low dopant activation and Fermi-level pinning, creating a barrier at metal/n-Ge junctions.

In one experiment, a 1000x increase in current was achieved by inserting a 0.7nm layer of n-ZnO between titanium metal and n-Ge (Figure 5). Specific contact resistance values ($0.8–1.5x10^{-6}\Omega$-cm^2) matching the best reported values on n-Ge have also been achieved. Increasing the doping of the n-Ge from $10^{19}/cm^3$ to $10^{20}/cm^2$ is expected to give the specific contact resistance of $10^{-8}\Omega$-cm^2 required by the International Technology Roadmap for Semiconductors (ITRS). ■

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