

# Record transconductance of 1105mS/mm for GaN/InAlN MIS-HFET

**UCSB has achieved maximum drain current density of 2.77A/mm in a gate-first self-aligned MIS-HFET device using N-polar nitride material.**

University of California Santa Barbara (UCSB) has produced gate-first self-aligned metal-insulator-semiconductor heterostructure field-effect transistors (MIS-HFETs) based on nitride semiconductors that demonstrated record extrinsic transconductance of 1105mS/mm [Nidhi et al, IEEE Electron Device Letters, published online 26 April 2012].

The devices used N-polar nitride semiconductor material rather than the more usual Ga-polar gallium nitride (GaN) buffer devices. Also, instead of a strained aluminium gallium nitride (AlGaN) top barrier, the UCSB devices use an unstrained indium aluminium nitride (InAlN) bottom/back barrier to generate a two-dimensional electron gas (2DEG) in the GaN channel layer.

The epitaxial material (Figure 1) for the devices was grown using plasma-assisted molecular beam epitaxy (PA-MBE) on C-face 6H silicon carbide (SiC) substrates. The  $\text{In}_{0.17}\text{Al}_{0.83}\text{N}$  back-barrier was lattice matched to the GaN layers. The 1nm of low-temperature GaN was designed to inhibit indium desorption in subsequent high-temperature process steps. The 2nm AlN inter-layer was aimed at reducing alloy scattering. The structure was found to give a low sheet resistance of 330 $\Omega$ /square.

A silicon nitride layer was applied as gate dielectric using metal-organic chemical vapor deposition (MOCVD). The gate metal stack consisted of tungsten/chromium/silicon dioxide/chromium. These steps constitute the 'gate-first' part of the self-aligned process.

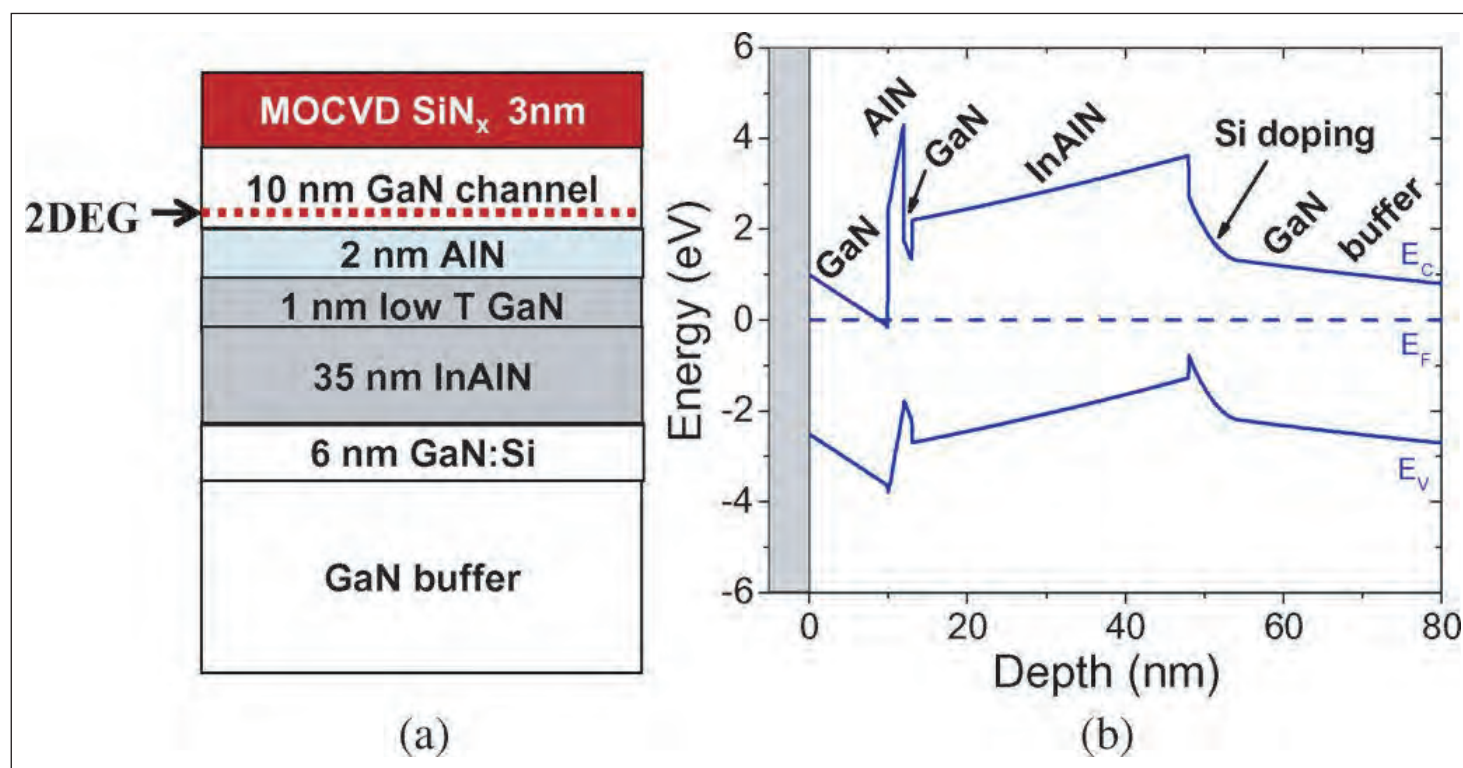


Figure 1. (a) Device epitaxial-layer structure for scaled GaN channel with an InAlN back barrier. (b) Band diagram of the device under the gate.

After gate definition, a 40nm layer of silicon nitride layer from plasma-enhanced chemical vapor deposition (PECVD) was used as spacer material around the gates to allow MBE re-growth of highly doped InGaN/InN for source/drain contact access, giving an 'ultra-low' contact resistance of  $25\Omega\text{-}\mu\text{m}$ . The polycrystalline growth on the gate finger was etched away, followed by mesa isolation of the individual transistor. Titanium/gold non-alloyed metal layers were used as source/drain ohmic and probe contacts.

A 60nm-gate device showed a maximum drain current density of  $2.77\text{A/mm}$  and an on-resistance of  $0.29\Omega\text{-mm}$ . The current is described as 'state-of-the-art' for both Ga-polar and N-polar devices. The on-resistance is "the lowest value ever reported for a GaN device."

At 0V gate potential, the saturated drain current was  $2.13\text{A/mm}$  at drain bias of 2V. For a 30nm-gate device, the saturated drain current density was  $2.25\text{A/mm}$ . The peak extrinsic transconductances ( $g_m$ ) were  $1105\text{mS/mm}$  and  $1000\text{mS/mm}$  for 60nm and 30nm gates, respectively. The researchers comment: "This is the highest value for extrinsic  $g_m$  reported for III-nitride

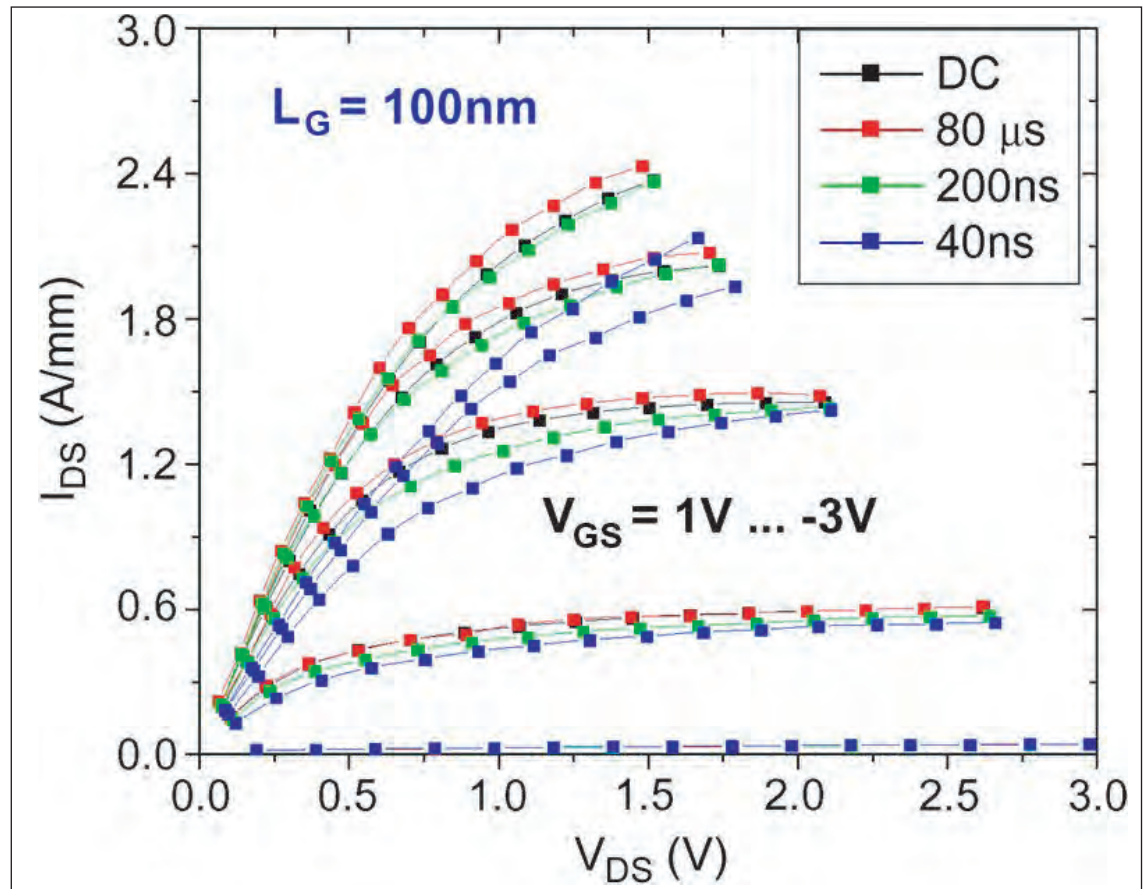


Figure 2. Pulsed current–voltage ( $I$ – $V$ ) characteristics for 100nm gate, showing significant current collapse and knee walkout for 40ns gate pulses.

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The off-state leakage was around  $20\text{mA/mm}$  for 2V drain bias. Hard breakdown occurred at 24V drain bias.

The researchers attributed the improved device performance to "significant reduction in the device to low on-resistance and high extrinsic transconductance."

The performance was also measured up to frequencies of 67GHz. The 30nm device had a cut-off frequency ( $f_T$ ) of 155GHz, but a maximum oscillation of only 20GHz (drain 3V, gate  $-2.5\text{V}$ ). The poor  $f_{\text{max}}$  figure was blamed on the high resistance of the tungsten-gate.

Although the  $f_T$  is 'excellent', it does not reflect what should be expected from the transconductance value, along with the relatively low values for the parasitic components. Pulsed measurements (40nsec), however, showed significant current collapse and 'knee walkout' (Figure 2).

The researchers tentatively attribute these effects to "shallow traps in the plasma MBE-grown InAlN or the low-temperature GaN layer below the AlN interlayer."

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