

AlN barrier enhancements to nitride HEMTs on silicon

France's Institute of Electronic, Microelectronic and Nanotechnology (IEMN) has published three reports of record performance for nitride semiconductor high-electron-mobility transistors (HEMTs) on silicon just in the last few months. Mike Cooke reports.

The next generation of millimeter-wave (mmW) power amplifiers could benefit from work at IEMN, where researchers are seeking to extend the frequency performance of nitride HEMTs on low-cost silicon substrates [1–3]. Already, an extrinsic cut-off frequency (f_T) and a maximum oscillation frequency (f_{MAX}) of 85GHz and 103GHz, respectively, have been achieved for one device [3].

These latest results also give high current (more than 2A/mm) and transconductance ($\sim 600\text{mS/mm}$) figures for the structure, along with the improved frequency characteristics. The DC performance is described as being "well beyond the highest reported values of any GaN-on-Si HEMTs".

The lead investigator Dr Farid Medjdoub reports on his attendance at the Device Research Conference (DRC, Santa Barbara, CA, USA, 20–22, June 2011) where he has recently presented the group's work: "As compared to the competitors (namely US labs), it appears that a key feature of this technology (beyond the record performances) is the possibility to maintain very low leakage current while aggressively down-scaling the device. The other research groups seem to struggle with gate leakage current with their short GaN devices and use a gate insulator to overcome this problem, which in essence degrades the DC and RF performance."

The IEMN devices all used ultrathin aluminum nitride (AlN) barrier layers to maximize carrier densities in the channel, reducing on-resistance (Figure 1). The use of AlN allows the barrier layer to be much thinner than normal (less than 10nm), bringing the gate much closer to the channel region. One of the devices developed by IEMN had a barrier as thin as 3nm [2].

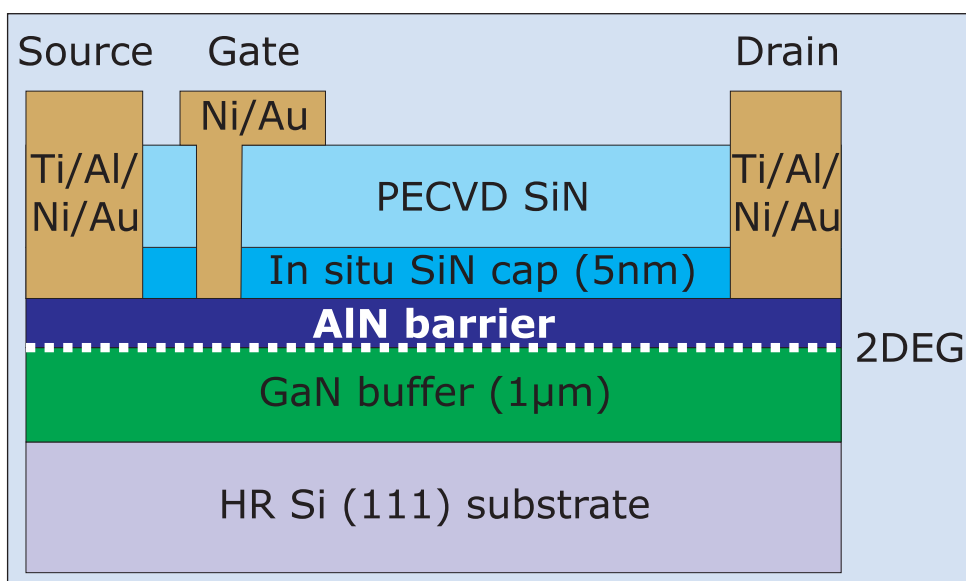


Figure 1. Schematic cross section of AlN/GaN-on-Si HEMTs fabricated by IEMN.

Nitride semiconductor material has a number of properties that makes it an attractive base for microwave power electronics applications. Among these characteristics, the large polarization charge can be used to create two-dimensional electron gases (2DEGs) with high carrier density and hence low resistance.

The wide bandgaps of nitride semiconductors also enable high power/current densities, and these materials' high thermal conductivity can be used to dissipate generated heat effectively. Improved breakdown voltages can also be expected.

In conventional nitride HEMTs, an aluminum gallium nitride (AlGaN) barrier layer is deposited on a GaN buffer, creating a 2DEG at the interface. As the barrier layer becomes thinner, the charge density decreases. Unfortunately, thinner barrier layers are needed to access high-frequency performance.

A further disadvantage is that thinner barriers make it more difficult to isolate the gate electrode from the channel, requiring the use of gate dielectric insulation,

Table 1. Physical dimensions of devices [1–3].

Ref.	AlN barrier (nm)	PECVD SiN (nm)	SiN passivation (nm)	Gate length (μm)	Gate-source (μm)	Gate-drain (μm)	Isolation implant
[1]	6	50	200	0.2	0.4	1.3	He
[2]	3	50	200	0.2	0.4	1.3	He
[3]	6	50	0	0.16	0.3	1.0	N

rather than a simpler Schottky contact, to reduce gate leakage currents. The processes used to apply dielectrics or to bring the electrode closer to the channel (e.g. recessing, where an etch process is used to make a slot in the barrier for the gate electrode) tend to degrade the reliability of devices.

High-aluminum-content barriers of indium aluminum nitride (InAlN) or even AlN, which has the highest spontaneous polarization of all the III-N materials, have lately been used to maximize 2DEG charge densities with promising results, suggesting useful performance up to W-band microwave frequencies (75–110GHz). Other groups use an AlN spacer layer, followed by AlGa_{0.3}N, to increase carrier densities in the 2DEG.

Another recent development in nitride semiconductors is their growth on large-diameter (up to 6 inch/150mm) silicon (Si) substrates, despite the challenge of a large lattice mismatch between the materials for high crystal quality. The achievement of nitride on Si suggests the possibility of low-cost — and hence large market adoption of — nitride semiconductor electronics.

EpiGaN (www.epigan.com) was commissioned to grow all the epitaxial material used on 4-inch (100mm) diameter (111)-oriented silicon wafers using metal-organic chemical vapor deposition (MOCVD). The substrates were highly resistive at more than 5000 Ω -cm. EpiGaN was spun-out of the IMEC European semiconductor research center in Belgium by Dr Stefan Degroote, Dr Joff Derluyn and Dr Marianne Germain (CEO).

Germain comments: "We are today able to provide GaN-on-Si epiwafer material for R&D or evaluation purposes, growing epilayer stacks upon specific customer request."

The epitaxial structures grown by EpiGaN for IEMN (Table 1) included a 5nm in-situ silicon nitride (SiN) layer that was designed to relax the high tensile stress in the AlN due to the large lattice mismatch with the underlying 1 μm GaN buffer. The stress relaxation prevents cracking of the surface, and reduces surface roughness. The in-situ SiN

also passivates surface charges that can deplete the 2DEG that forms in the barrier-buffer interface region, needed for channel conduction. The researchers further believe that the in-situ SiN layer enhances the surface robustness of the high-quality AlN barrier, avoiding gate tunneling under high electric field.

Room-temperature Hall measurements on epitaxial material with a 6nm AlN barrier on a GaN buffer gave an electron sheet density of $2.15 \times 10^{13}/\text{cm}^2$ and a mobility of $1250\text{cm}^2/\text{V-s}$ [1, 3]. By contrast, the traditional AlGa_{0.3}N barrier 2DEG carrier density becomes less than $10^{13}/\text{cm}^2$ for thicknesses less than 10nm. Although lattice-matched In_{0.17}Al_{0.83}N has much better performance in this respect than AlGa_{0.3}N, it is beaten by AlN at all barrier thicknesses less than 10nm (Figure 2). The mobilities of the AlN 2DEGs were in the range 1100 – $1550\text{cm}^2/\text{V-s}$.

An ultrathin barrier layer of 6nm is less than the critical thickness of 9nm above which the crystal quality of AlN epitaxial layers degrades, but it is still subject to a high amount of tensile stress due to the lattice mismatch between AlN and GaN. ▶

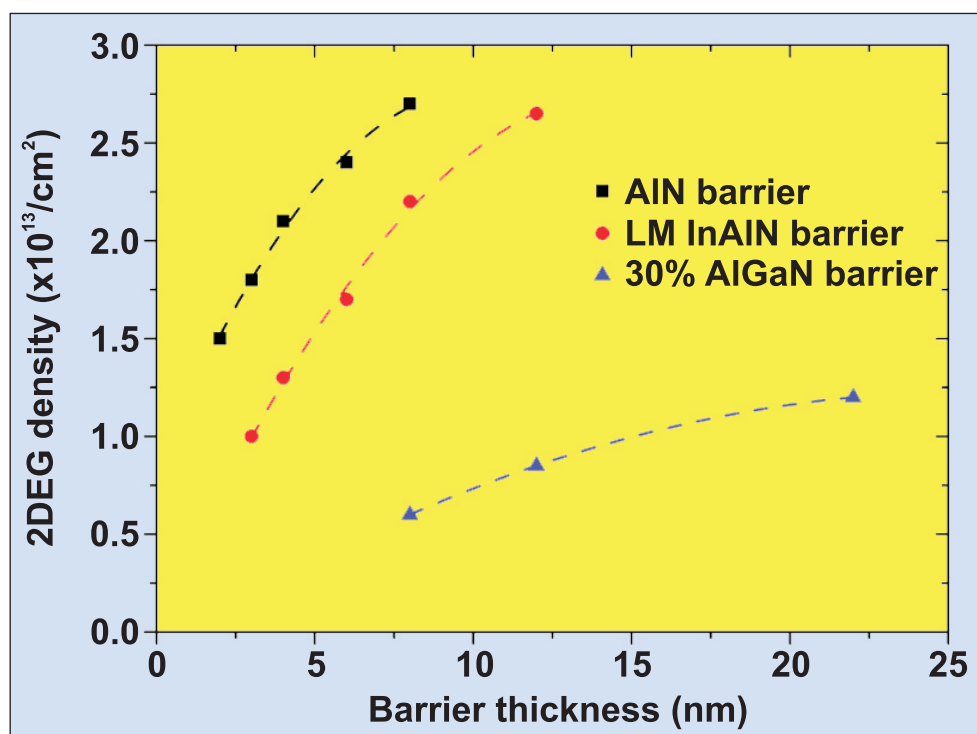


Figure 2. Room-temperature 2DEG carrier density measured by van der Pauw method of SiN/AlN/GaN, lattice matched In_{0.17}Al_{0.83}N/GaN, and Al_{0.3}Ga_{0.7}N/GaN heterostructures as a function of barrier layer thickness.

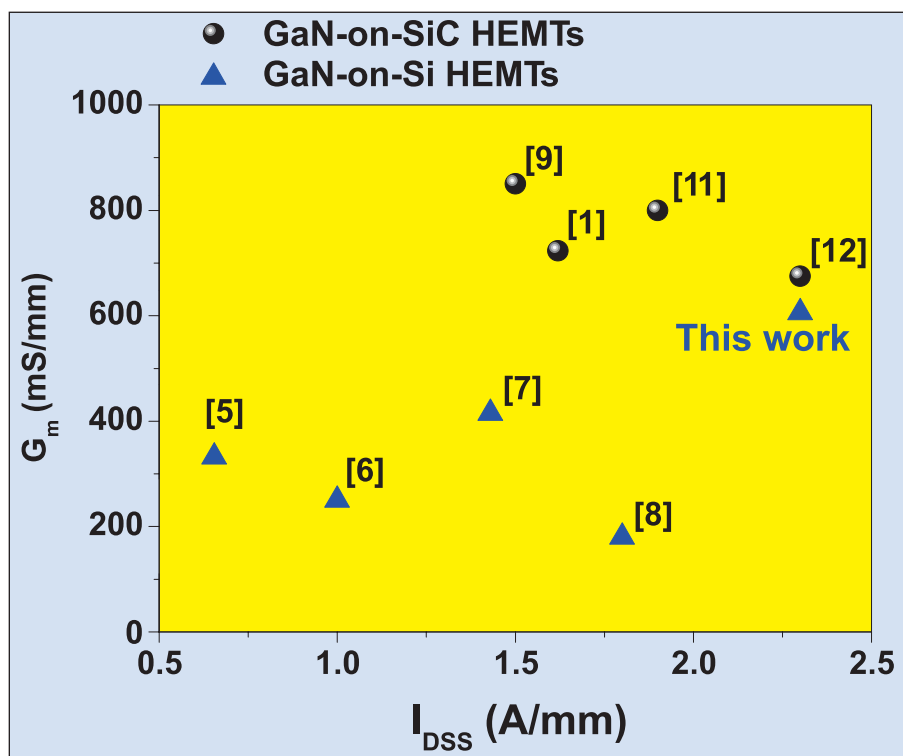


Figure 3. Benchmarking of extrinsic transconductance as a function of maximum saturated current density (I_{DSS}) of GaN-on-Si HEMTs (blue triangles) and GaN-on-SiC HEMTs (black circles).

► Medjdoub credited the better results of the latest work [3] on “process improvement” in the construction of the HEMT devices. The Ohmic source–drain contacts consisted of titanium–aluminum–nickel–gold (Ti/Al/Ni/Au), deposited on the AlN barrier material after etching through the SiN layer. The ohmic metal layers were then subjected to rapid thermal annealing (RTA) at 850°C for HEMT [3]. Nitrogen was implanted to isolate devices.

The earlier devices [1, 2] were isolated using helium implantation, and the annealing was performed at 900°C in nitrogen ambient. The ohmic contacts in [3] achieved a lower contact resistance of 0.4Ω–mm, compared with the 0.65Ω–mm of [1, 2]. Forming Ohmic contacts on AlN can be particularly tricky (see e.g. www.semiconductor-today.com/news_items/2011/JULY/MITSUBISHI_020711.html).

More silicon nitride was then deposited in devices [1, 3] using plasma enhanced chemical vapor deposition (PECVD), before gate formation. The nickel–gold (Ni/Au) gate was deposited after photolithography and etching through the SiN with sulfur hexafluoride

plasma that has a SiN/AlN selectivity factor of 90.

The gate length of the new device [3] was smaller than before [1, 2] (Table 1) at 0.16μm with gate–source and gate–drain distances of 0.3μm and 1μm, respectively. The device width was kept at 50μm. The earlier devices [1, 2] had an extra 200nm PECVD SiN layer that was added as further passivation.

The maximum DC output current density for the new device [3] was 2.3A/mm, “reflecting the high sheet carrier density provided by the AlN material that possesses the highest spontaneous polarization among all III–nitrides.”

Current densities up to 2.3A/mm were also seen in device [1] (Table 2), but only under pulsed operation (500ns, 1% duty cycle). The difference in behavior between the DC (2.03A/mm) and pulse maxima was attributed to the limited thermal dissipation of the silicon substrate when the device is subjected to direct current. The researchers also reported slight gate and drain lag effects in [1] due, it

was thought, to damage from the gate etch process that needed to be further optimized.

Leakage was also investigated using various structures. Under reverse bias of the Schottky diode gate, where the current should be small, the gate leakage was found in [3] to be less than 100μA/mm up to 80V. Buffer leakage, which was determined using a separate structure with two isolated ohmic contacts having 5μm spacing on the material, was less than 4μA/mm up to 200V bias.

The extrinsic transconductance of device [3] had a peak value of 606mS/mm at a –1.6V gate potential and a source–drain bias of 4V. The transconductance was more than 500mS/mm for V_{DS} in the 2–6V range under the same gate potential. This performance puts the device into comparison with GaN HEMTs on expensive silicon carbide that benefit from smaller lattice mismatch (and hence better nitride crystal quality, giving an improved 2DEG) and the high thermal conductivity of the substrate reducing self-heating effects (Figure 3).

Frequency performance measurements were also carried out (Figure 4), giving an extrinsic cut-off fre-

Table 2. Electrical performance summary.

Ref.	Output current density (A/mm)	Peak transconductance (mS/mm)	f_T (GHz)	f_{MAX} (GHz)	$f_T \cdot L_g$ (GHz–μm)
[1]	2.03	390	52	102	10.4
[2]	1.3	470	—	—	—
[3]	2.3	606	85	103	13.6

quency (f_T) and a maximum oscillation (f_{MAX}) frequency of 85GHz and 103GHz, respectively. These are high figures, given the “relatively high access resistances and residual losses most probably located at the buffer/Si substrate interface”. The high lattice mismatch between the buffer and silicon substrate is blamed for a 0.7dB/mm loss at 50GHz in coplanar waveguide measurements.

The cut-off-gate length product ($f_T \times L_g$) of 13.6GHz- μm suggests that downscaling the gate length to less than 100nm “will allow very high-frequency operation considering the high aspect ratio achievable with sub-100nm gate lengths.” The previous device [1] had a cut-off-gate length product of 10.4GHz- μm with an f_T of 52GHz and an f_{MAX} of 102GHz (Table 2). These cut-off-gate length products are favorably comparable to reported state-of-the-art GaN-on-Si HEMTs with 80nm gate length.

Medjdoub reports that IEMN is acquiring a 40GHz-input power amplifier to be able to fully characterize the high-power performance at higher frequency of his group’s devices.

The researchers conclude: “The high-frequency performance achieved for a gate length of 0.16 μm promises breakthrough millimeter-wave low-noise and high-power monolithically integrated amplifiers in a cost-effective way.” ■

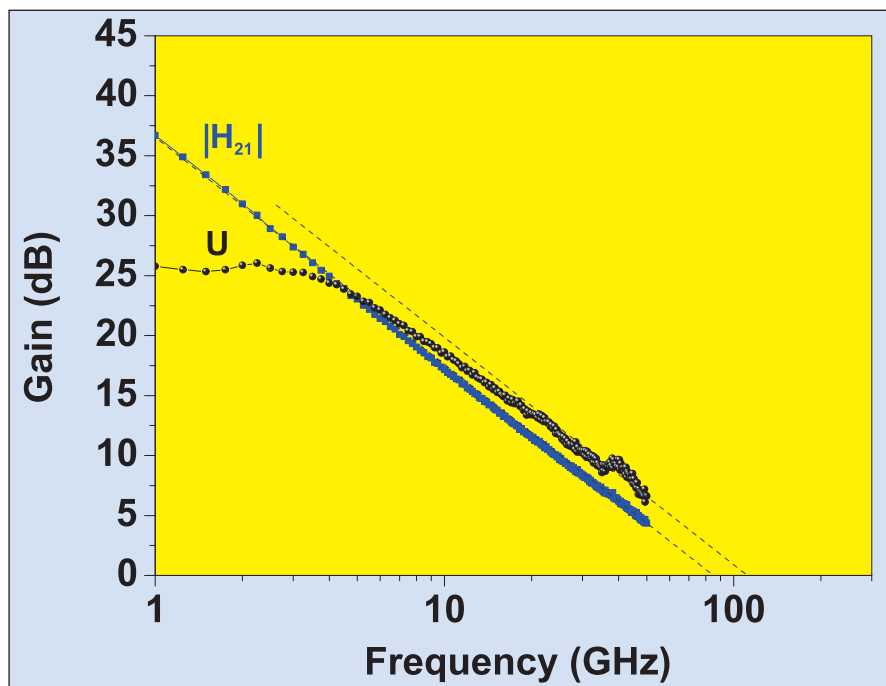


Figure 4. RF performance of 0.16 μm x 50 μm AlN/GaN HEMT on highly resistive silicon substrate. Extrapolation at -20dB/dec yields f_T of 85GHz and f_{MAX} of 103GHz at V_{DS} 4V and V_{GS} -1.6V.

Mike Cooke is a freelance technology journalist who has worked in semiconductor and advanced technology sectors since 1997.

References

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