Making III-V contact with silicon substrates

High-speed logic, high-frequency/high-power transistors and photonics systems could benefit from marrying with silicon substrates. One impediment to this is contact formulations that use gold. Researchers are working to find a way to union through gold-free contacts. Mike Cooke reports.

There has been a recent push to integrate III-V materials with silicon complementary metal oxide semiconductor (CMOS) field-effect transistor (FET) logic. This push is aimed in three directions: high-mobility channels for logic transistors, high-frequency/high-power nitride semiconductor devices, and photonics systems.

Indium gallium arsenide (InGaAs) is the main material being developed with a view to enhancing the performance of the CMOS logic circuits that are at the base of present day electronics. In particular, as these devices become smaller, the electronic properties of silicon are insufficient to overcome a series of 'short-channel effects'. InGaAs is attractive because it has a much higher mobility than silicon. InGaAs could also be used to produce photonic devices that detect and emit light into silicon-based waveguides with CMOS-controlled elements such as optical attenuators.

Further, since the development of gallium nitride (GaN) layers on silicon, researchers have considered the possibility of developing integrated devices combining the high-frequency/power/temperature capabilities of nitride semiconductors with the logic versatility of high-performance silicon electronics. A particular attraction is the commercial availability of 6-inch (150mm) GaN-on-silicon wafers that could be used in fabrication facilities originally designed for silicon devices such as silicon-based power transistors.

The road to such integration is not straightforward but has many problems that are being intensively worked on by researchers. One hurdle to overcome in this is the use of gold in producing ohmic connections to the source and drain (S/D) regions of III-V field-effect transistors, both for InGaAs (Table 1) and for nitride semiconductors.

The problem is that gold is 'banned' in silicon device fabrication, since gold produces acceptor and donor levels in silicon that poison device performance. Copper is another CMOS poison. However, copper has found use in CMOS wiring in high-performance and/or low-power devices, although the metal has to be carefully separated from the CMOS layers with barriers consisting of materials such as tantalum or tantalum nitride.

Table 1. Possible contact materials for InGaAs devices.

Material system	N_c(cm^{-3})	ρ_c(Ω-μm^2)	Type
Mo	$3.6x10^{19}$	1.3	n
Ni/Au-Sn/Ni	$2.2x10^{18}$	4	n
AuGe	$2.2x10^{18}$	8	n
Au-Ge-Ni	$1x10^{17}$	50	n
Au/Pt/Ti	$3x10^{19}$	20	n
Pd/AuGe	$2.3x10^{19}$	40	n
Au/Sn/Au	$3x10^{19}$	30	n
Ni/Au-Zn/Ni	$1.5x10^{18}$	2000	p
Au/Pt/Ti	$2x10^{19}$	1100	p
Pt/Ti	$5x10^{18}$	900	p
Pd/AuGe	$4x10^{19}$	400	p
AuBe/Pt/Au	$2x10^{19}$	750	p

The presence of gold in the typical nitride semiconductor ohmic metal layer stack titanium/aluminum/XY/gold (Ti/Al/XY/Au) is thought to improve the contact resistance by creating gallium vacancies in the nitride semiconductor material and by preventing oxidation of the stack by the atmosphere. The XY-layer is a diffusion layer (typically nickel, palladium or molybdenum). On the negative side, long-term gold diffusion has also been associated with degradation of the ohmic contacts. This latter possible effect gives another motivation for developing gold-free set-ups.

For nitride devices, selective doping of the S/D contacts has been attempted in creating gold-free processes, but these methods tend to reduce breakdown voltages and increase leakage currents. Complicated regrowth methods have also been tried — however, these would be expensive to implement in manufacturing.

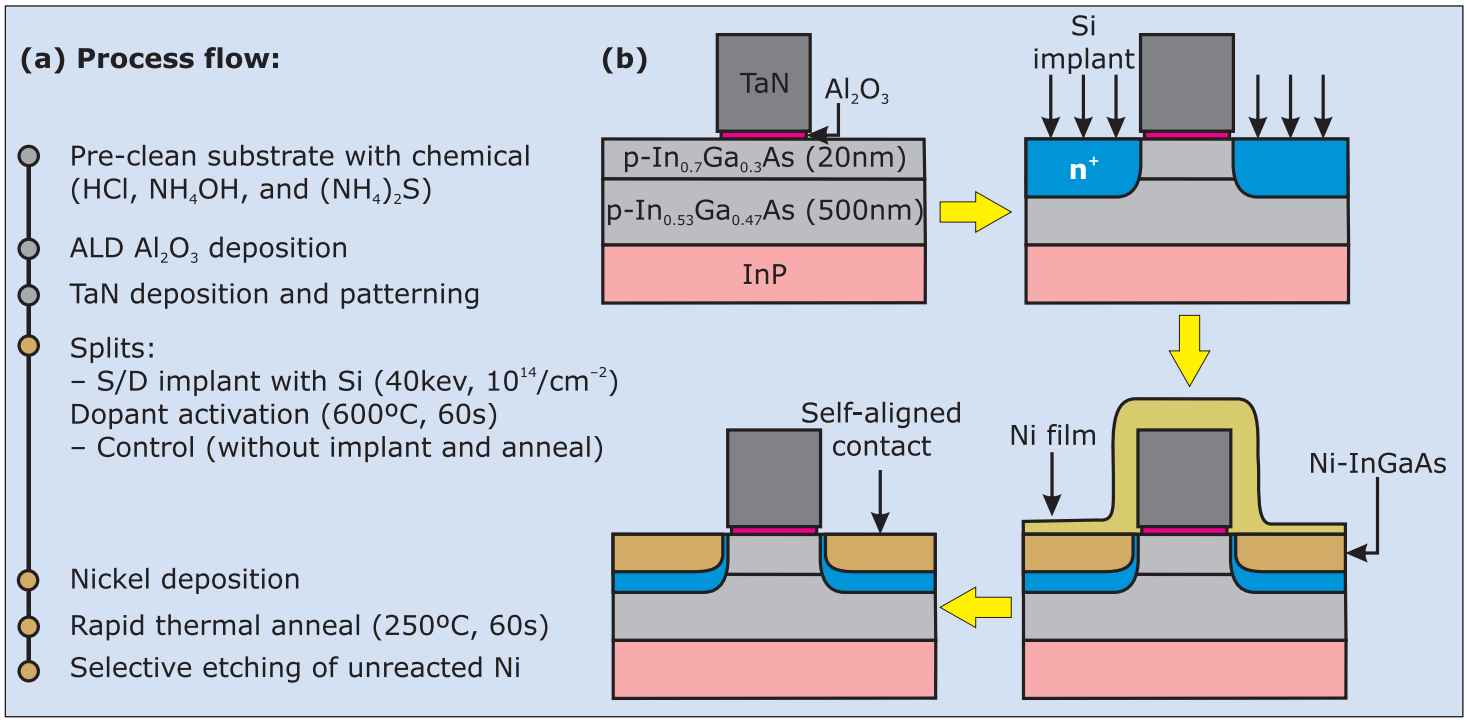

Figure 1. (a) Process flow for fabrication of $In_{0.7}Ga_{0.3}As$ n-MOSFETs with self-aligned Ni-InGaAs contacts and metal S/D. (b) The salicide-like metallization process comprises a reaction of Ni with $In_xGa_{1-x}As$ and a selective removal of excess Ni using a wet etch.

Self-aligned InGaAs

With InGaAs MOSFETs, it is hoped to mimic silicon CMOS processes that presently use a self-aligned silicide ('SAlicide') S/D process. The self-alignment uses previously patterned structures rather than a separate lithographic process (that would require precise alignment) to form the S/D contact regions.

National University of Singapore (NUS) and Taiwan Semiconductor Manufacturing Company (TSMC) claim the first demonstration of self-aligned nickel (Ni) source/drain contacts for InGaAs n-MOSFETs [Xingui Zhang et al, Electrochemical and Solid-State Letters, vol14 pH60, 2011, published online 19 November 2010].

Ideally, source/drain contacts should be ohmic. The reaction of the Ni with InGaAs during rapid thermal annealing creates a material with sheet resistance of 20Ω/square. The contact is found to be ohmic in the case of Ni annealed with n-InGaAs, while a Schottky (rectifying) contact is formed with p-InGaAs.

"This work (and that of others along similar lines) suffered from high off-state leakage current and a relatively low on-state to off-state current ratio," says one of the leaders of this research, Dr Yee-Chia Yeo. "This problem has been resolved in our follow-up work [Xingui Zhang et al, International Symposium on VLSI Technology Systems and Applications, Session 2, T24, 25 April 2011]. In this new work, an n^+ implanted region is introduced beneath the self-aligned Ni-InGaAs regions to suppress the off-state leakage current."

NUS/TSMC's salicide-like metallization process for Ni-InGaAs contacts (Figure 1) begins with surface preparation and atomic layer deposition (ALD) of aluminum oxide (Al_2O_3) gate dielectric/insulator on the epitaxial InGaAs layers on indium phosphide (InP) substrates. The gate electrode consisted of tantalum nitride (TaN). A spacer was not used.

The application of a silicon implant step before the source/drain metallization was found to reduce the OFF-state current by a factor of 10 (Figure 2). The

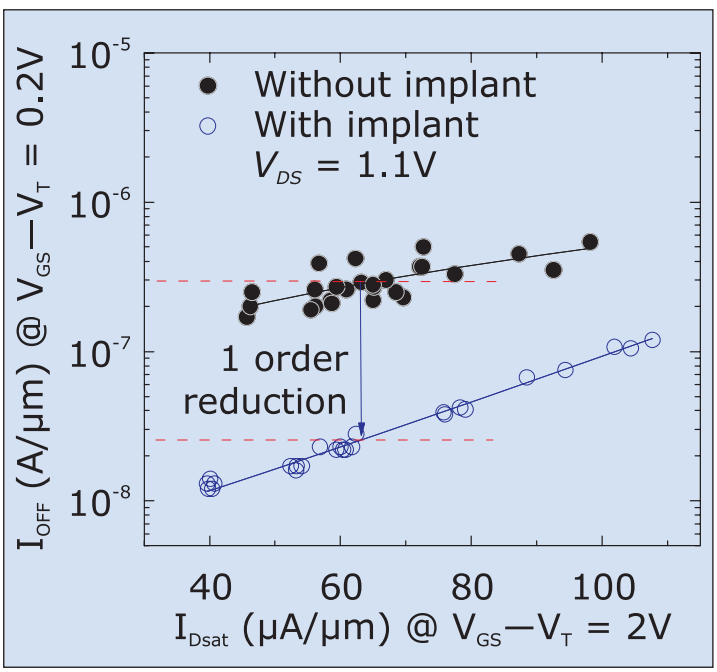

Figure 2. Devices with a source/drain (S/D) implant show a reduction of over one order of magnitude in the OFF-state current (I_{OFF}) in the saturation regime.

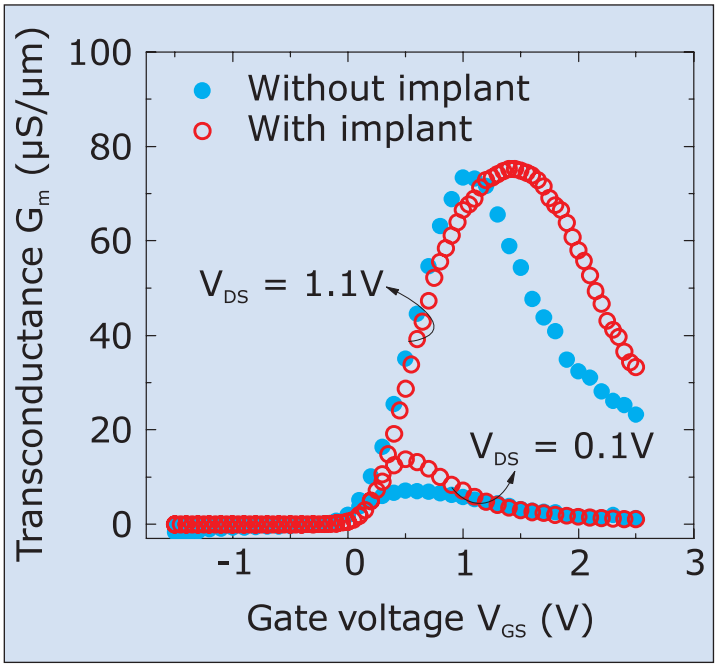

Figure 3. Transconductance–gate potential (G_m–V_{GS}) curves for devices with and without silicon implant of S/D regions. Slight G_m enhancement was observed for device with S/D implant.

implant also gave a slight enhancement to the transconductance (Figure 3) due to a 16% reduced S/D resistance (median values). The median sub-threshold swing was also reduced by 19% for the implanted devices (from a high value of ~250mV/dec).

The n-MOSFETs reported last year had a gate length of 1μm and demonstrated an on-state/off-state drain current ratio of ~10^3 and peak transconductance G_m of 74μS/μm. Earlier last year some of the same researchers used a nickel germanium formulation to produce the first CMOS-compatible III-V n-MOSFET with self-aligned contacts [reported at www.semiconductor-today.com/news_items/2010/JUNE/VLSI_180610.htm and Semiconductor Today, June/July 2010, p83].

Scientists variously based at University of Tokyo, National Institute of Advanced Industrial Science and Technology (NAIST), Sumitomo Chemical Co Ltd have also developed a self-aligned Ni-InGaAs alloy S/D process for application in InGaAs nMOSFETs [SangHyeon Kim et al, Appl. Phys. Express, vol4, p024201, 2011; reported www.semiconductor-today.com/news_items/2011/FEB/NAIST_040211.htm and Semiconductor Today, February 2010, p104]. With an $In_{0.7}Ga_{0.3}As$ channel, the device achieved an on/off current ratio of 10^4 and subthreshold slope of 147mV/dec (a low figure indicates a desirable sharp turn-on of current). Other III-V devices have achieved 120mV/dec and better. Silicon CMOS can achieve about 70mV/dec, near to the theoretical limit of 60mV/dec for planar structures.

In work presented at IEDM [Semiconductor Today Dec/Jan 2010/2011, p100], the US-based SEMATECH industry research consortium reported on Al/TiN contacts, obtaining a source–drain resistance value of 1880.8Ω-μm, which the researchers believe is consistent with a sheet resistance of 300Ω/square and a contact resistance 10^{-6}Ω-cm^2. An improved contact resistance of 10^{-8}Ω-cm^2 (1Ω-μm^2) has been achieved in experiments, the details of which have yet to be published by SEMATECH.

For InGaAs photonics, the European Union framework 7 (FP7) projects Wavelength Division Multiplexed Photonic Layer on CMOS (WADIMOS, www.wadimos.eu) and pHotonics ELectronics functional Integration on CMOS (HELIOS, www.helios-project.eu) have supported work on gold-free contacts for InP-based photonics devices on silicon. In one France-based study [L. Grenouillet et al, 'CMOS compatible contacts and etching for InP-on-silicon active devices', Group IV Photonics conference, San Francisco, 9–11 September 2009], Ni/Al and Ti/Al were used as ohmic contacts on n-InP, giving contact resistance values of $2x10^{-5}$Ω-cm^2 and $5x10^{-5}$Ω-cm^2, respectively, without annealing. A CMOS-style Ti/TiN/AlCu stack was also investigated, giving contact resistances of $1x10^{-4}$Ω-cm^2 on n-InP and $6x10^{-5}$Ω-cm^2 on p-InGaAs, again without annealing.

Gold-free nitrides

For nitrides, Massachusetts Institute of Technology (MIT) has recently developed gold-free ohmic contacts on high-electron-mobility transistors (HEMTs) on silicon substrates with performance close to that of traditional contacts containing gold [Hyung-Seok Lee et al, IEEE Electron Device Letters, published online 20 March 2011].

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The MIT researchers used 4-inch (111)-oriented silicon wafers (100mm diameter) on which nitride semiconductor layers had been grown (Figure 4) using metal-organic chemical vapor deposition (MOCVD): the undoped GaN buffer layer was 1.8μm thick; the aluminum gallium nitride (AlGaN, with 26% Al) barrier and undoped GaN cap layers were 17.5nm and 2nm, respectively.

The mesa isolation and recessing were carried out using electron cyclotron resonance (ECR) etching with boron trichloride/chlorine plasma. The metal contact stack was deposited using electron-beam evaporation. The gold-free stack consisted of titanium (Ti), Al and tungsten (W). The final tungsten layer forms a barrier to prevent oxidation of the Al. ►

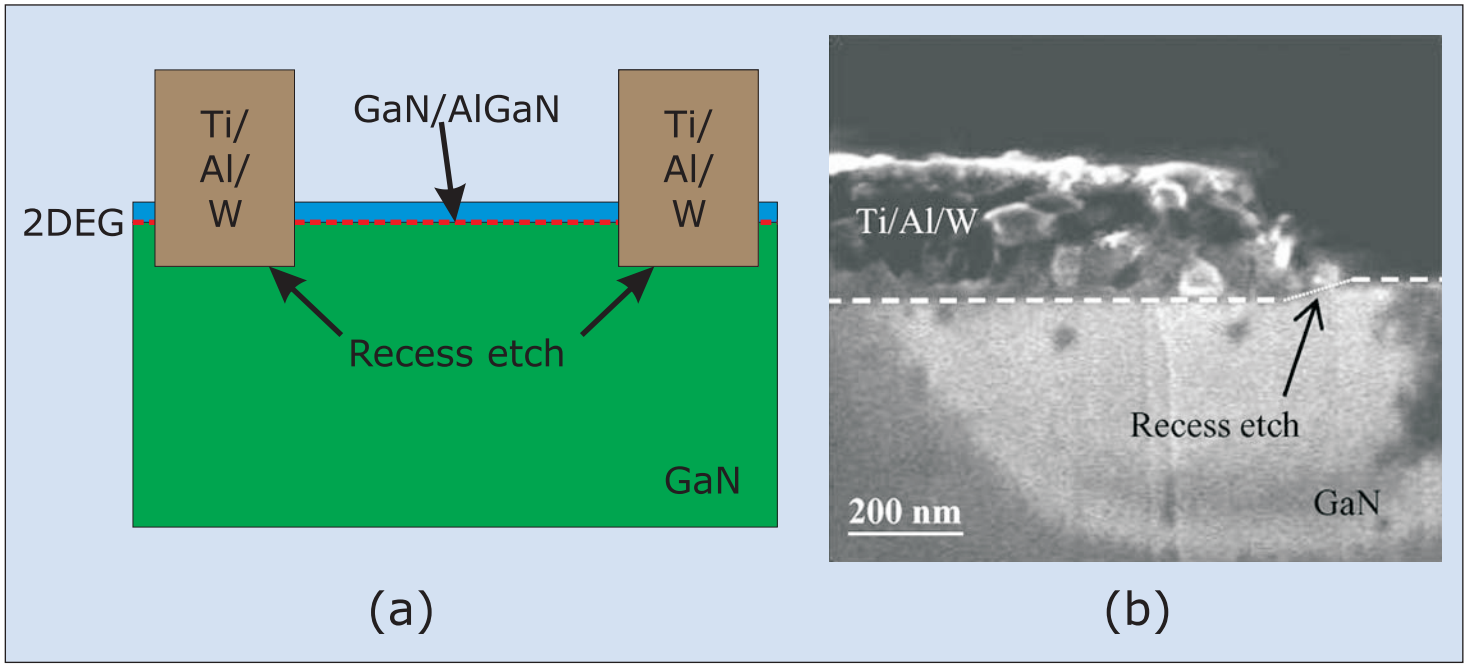

Figure 4. (a) Schematic cross section of the fabricated undoped AlGaN/GaN HEMTs with S/D ohmic recess. (b) SEM image of the cross section of a Ti/Al/W contact after annealing. Before metallization, the ohmic contact region was recessed ~30nm.

Rapid thermal annealing was used with a temperature of 600–1000ºC. It was found that annealing at more than 800ºC (900ºC for samples without recess) was needed to give linear ohmic behavior.

Various recessing depths were tried: 0nm (i.e. no recessing), 15nm and 30nm. A gold-based stack (titanium-aluminum-nickel-gold) was also produced as a control sample. The lowest contact resistance for the gold-free set up was obtained with 30nm recessing: 0.49Ω-mm with 870ºC anneal. The best results for no- and 15nm-recessing were 2.02Ω-mm (950ºC anneal) and 1.71Ω-mm (870ºC). The anneal times for these results were 30 seconds.

The full recessing of 30nm puts the ohmic metal stack in contact with the two-dimensional electron gas (2DEG) that forms the channel of the nitride semiconductor HEMT. It is also thought that formation of nitrided Al and Ti after annealing reduces the energy barrier between the contact metal and 2DEG.

Specific contact resistances were measured using linear transmission line method (LTLM) structures (Figure 5a). The Ti/Al/W stacks with (30nm) and without recessing had specific contact resistances of 6.5×10^{-6}Ω-cm^2 and 8.7×10^{-5}Ω-cm^2, respectively. The value for the control Ti/Al/Ni/Au contact annealed at 870ºC was 3.1×10^{-6}Ω-cm^2. The contact resistance for the control was 0.38Ω-mm.

The researchers also studied the surface smoothness (Figure 5b) of the various contacts (morphology). The gold-free contact (Ti/Al/W) was much smoother, due, it is thought, to the absence of $AuAl_4$ alloys. Such smoothness is an advantage in highly scaled (i.e. ultra-small) devices.

Apart from the source–drain ohmic contact structures, all samples underwent nominally the same epitaxial and fabrication processes.

After the source–drain contacts had been formed, the gate structure (3nm Ga_2O_3 dielectric, Ti/Al/W metal electrode stack) was formed and 20nm Al_2O_3 passivation was applied using atomic layer deposition. The Ga_2O_3 dielectric was formed by exposing the gate region to oxygen plasma.

The produced transistors had gate lengths of 3μm. The gate–source and gate–drain distances were both 1.5μm. All the devices had a threshold voltage of about –2.2V (depletion-mode, normally-on), gate leakage less than 10mA/mm and 87V three-terminal breakdown (at a gate potential of –6V).

However, the 100mA/mm on-current behavior was much improved through recessing with a source–drain voltage drop of only 0.78V, rather than the 1.31V needed for the non-recessed sample. The traditional gold-based contacts had a 0.68V drop at the same current level. The recessed contacts therefore have only a 15% increased voltage compared with the traditional ohmic structure. Since the devices are 'normally-on', the gate potential in these measurements is zero.

The researchers conclude: "These results enable the fabrication of high-performance GaN power devices in Si fabs without the risk of contaminating the Si wafers, which enables the large-scale production of GaN power electronics."

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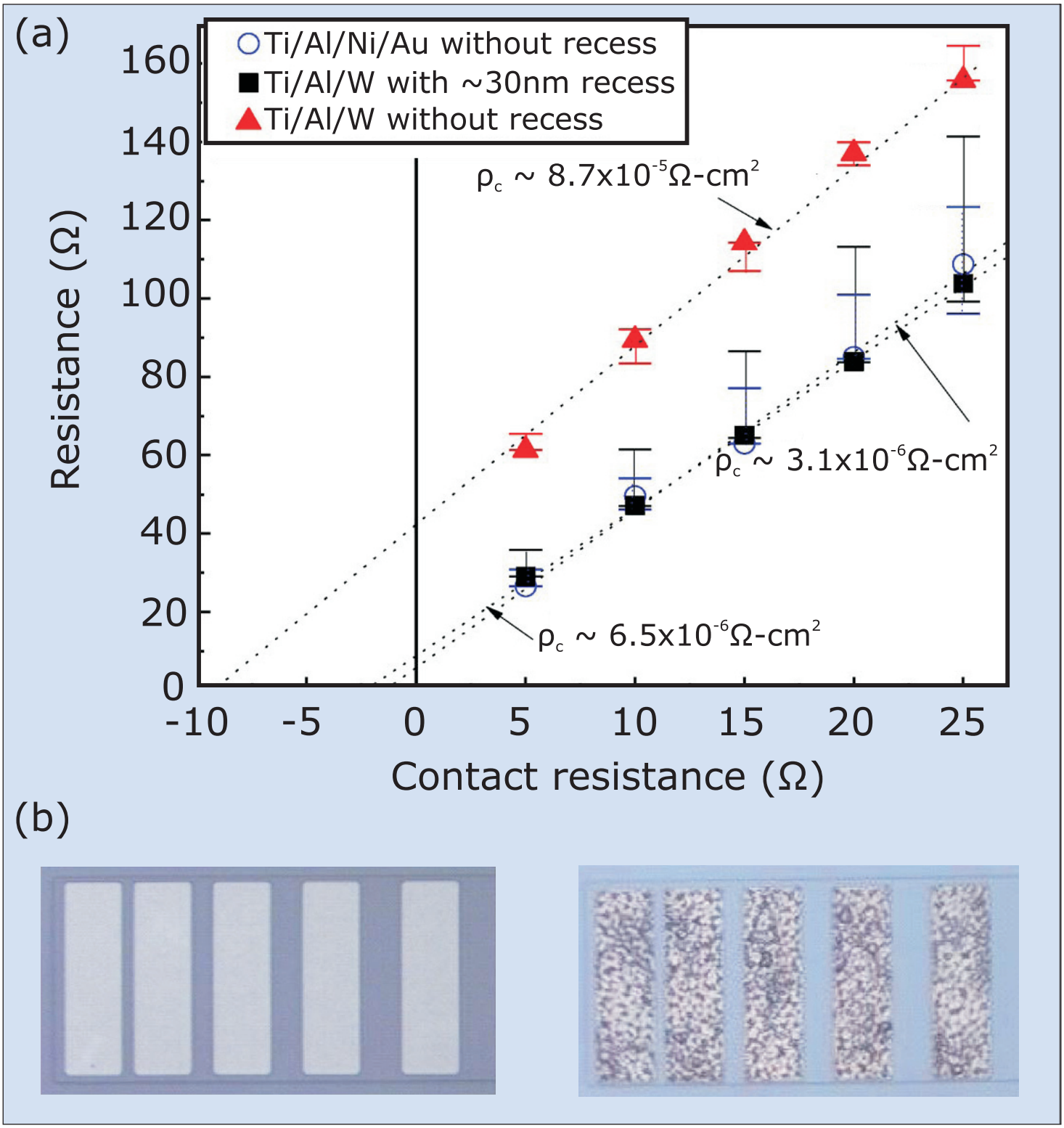

Figure 5. (a) Total resistance for different ohmic metallization processes as a function of contact distance. (b) Optical micrograph images of the surface for (left) Ti/Al/W recessed contacts and (right) standard Ti/Al/Ni/Au contacts.

Another recent report of gold-free source–drain contacts for nitride HEMTs comes from Sweden's Chalmers University of Technology and France/Germany-based United Monolithic Semiconductors (UMS) [A Malmros et al, Semicond. Sci. Technol., vol26, p075006, 2011; see separate report this issue]. Although this research was not directed towards nitride HEMT integration with silicon, the researchers compared a traditional Ta/Al/Ni/Au metallization scheme with a gold-free Ta/Al/Ta formulation that might be of interest in such work. ■

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