Enhanced BiFET boosts

Skyworks' Ravi Ramanathan and colleagues detail how the BiFET process is integrated into a high-volume GaAs HBT manufacturing facility, allowing integration of external bias control circuitry into wireless power amplifier die.

Handset designers continue to strive for higher levels of integration in order to reduce the size and cost of next-generation products while improving battery life. One key integration target for the industry has been the incorporation of external bias control circuits into the power amplifier (PA) die. This is now possible using enhanced bipolar field effect transistor (BiFET) process technology for gallium arsenide-based products. BiFET technology uniquely integrates indium gallium phosphide-based heterojunction bipolar transistors (HBTs) with field effect transistors (FETs) on the same GaAs substrate using a high-yielding InGaP/GaAs HBT process. This article will explore the manufacturability requirements of this innovative BiFET process technology that opens up new opportunities to embed analog signal processing and control functionality in mobile handsets as well as infrastructure wireless applications.

The addition of FETs to Skyworks' fourth-generation, high-yielding InGaP/GaAs HBT process allows advanced bias control features to be embedded in the same PA die, thereby eliminating the need for external bias control circuits for many applications. When coupled with other proprietary design techniques that extend battery life and reduce the radio-frequency loss between integrated components, semiconductor manufacturers are able to increase functionality and simplify designs while leveraging production costs across a suite of GaAs-based solutions, and address additional markets that require embedded analog signal processing and control functionality.

Several BiFET integration schemes have been proposed and demonstrated by a variety of research groups [1-4]. To establish a BiFET process in Skyworks' high-volume GaAs HBT production line, we have evaluated some of these possible BiFET integration approaches and found most of these methods have drawbacks with respect to high-volume manufacturing. Due to Skyworks' stringent yield requirement in a cost-conscious environment, a hybrid BiFET approach, achieved through a single epitaxial growth run, was selected and developed.

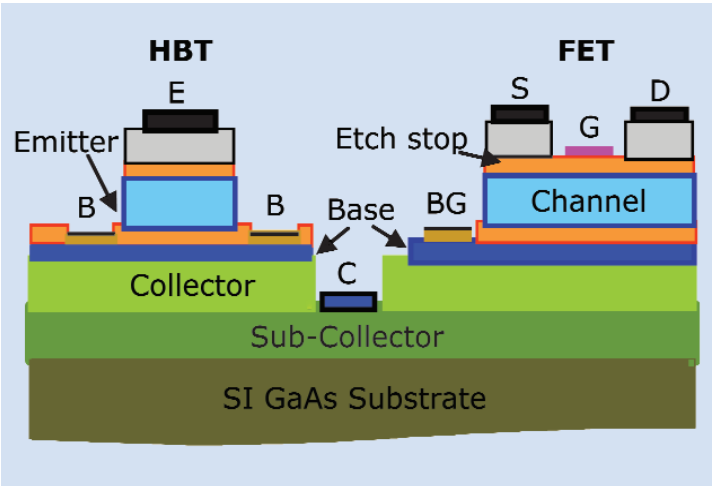

Figure 1: Schematic cross section of an integrated HBT and FET. S, D, G and BG are the source, drain, gate and back-gate contacts of the FET, and E, B and C are the emitter, base and collector contacts of the HBT.

Material growth and device fabrication

Epitaxial layers, consisting of the InGaP emitter, base and collector of the HBT, are grown on semi-insulating (SI) GaAs (100) by using metal organic chemical vapor deposition (MOCVD). The FET-specific layers such as the channel and an optimized etch stop layer are grown within the emitter of the HBT. A schematic cross-sectional profile of the BiFET layer scheme is shown in Figure 1.

In a high-volume GaAs HBT manufacturing environment, the starting epitaxial materials should be 'pre-screened' and sufficient quantities need to be kept in material inventory or in consignment for uninterrupted lot starts. A quick-lot (QL) process is often used by material suppliers to ensure that the incoming HBT wafers meet the desired specifications. Typically, large-area (75μm x 75μm) HBT devices are fabricated and electrical parameters such as direct-current gain, offset voltage, base–emitter/base–collector turn-on voltages, sheet resistances, and junction breakdown voltages are measured from multiple sites on a witness wafer. However, since FET devices are sensitive to process conditions, electrical measurements such as pinch-off voltage, saturation current and transconductance vary significantly due to the process and mask the growth variations. Hence, the FET QL process and electrical characterization of FETs, at the material

wireless integration

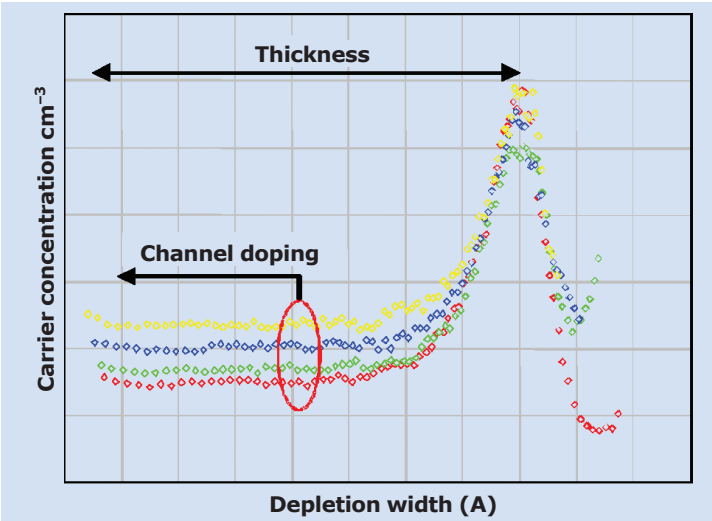

Figure 2: C–V profile of emitter layer stack in a BiFET wafer. Various curves are collected from design of experiment wafers with various doping concentrations.

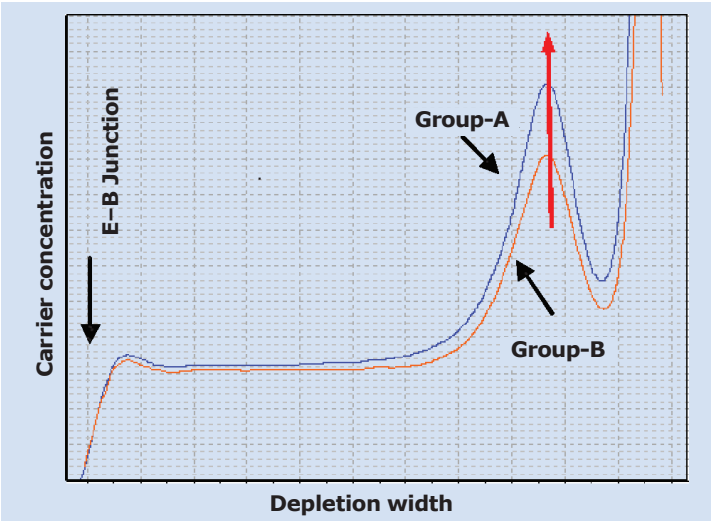

Figure 3: C–V profiles of the emitter–base (E–B) junction of BiFET wafers. Group A wafers and Group B wafers come from different MOCVD growth runs.

supplier sites, are often inadequate to screen the quality of the epitaxial layers.

In addition, an alternate FET QL procedure should also be simple to interpret, faster, and depend only on run-to-run and machine-to-machine growth variations. To this end, in collaboration with the epi supplier, a capacitance–voltage (C–V)-based QL procedure has been established. Figure 2 illustrates a typical emitter–base junction C–V profile collected from a set of design of experiment (DOE) wafers with different doping concentrations. From the C–V profile, one can extract the FET channel thickness and doping concentration, as depicted in Figure 2. Using this simple characterization technique, consistent thickness and doping information have been obtained to establish a correlation with the FET electrical parameters that are acquired after full wafer fabrication. Failure to implement such QL strategy can result in very costly yield issues and potential scraps at the end of the line.

In defining the FET, the challenge is to add a minimum number of masking steps to define the channel and gate regions, and these FET-specific process steps have to be introduced into the HBT flow at the appropriate steps and still preserve the electrical integrity of the FET and HBT devices. The source and drain contacts of the FET share the same fabrication steps that are used to form the emitter contacts of the HBTs. In placing the gate metallization step, care should be taken to limit the exposure of gate metal Schottky contact to high temperatures (>300°C) and longer isothermal anneal cycles. FET device-to-device isolation is achieved by the combination of dry etch and ion implantation process, both of which are used in the definition of the HBTs.

Influence of fabrication steps on FETs

To achieve the goal of high yield for FETs, similar to that of HBTs, the following process variations must be studied and controlled:

Epitaxial variation

The implication of run-to-run growth variation on the C–V profile and the correlation to FET pinch-off voltage is shown in Figures 3 and 4. From the C–V profile, one can infer that the bulk channel doping and channel thickness of the two groups of wafers are the same.

However, the charge difference between the groups, as shown in Figure 3, could be the result of either charge build-up at the interface of the etch-stop layer and the channel layer and/or the doping in the etch-stop layer, which results in a shift of 100 mV in the pinch-off voltage, as shown in Figure 4.

Gate definition process

The metal–semiconductor FET in BiFET technology consists of a thin etch-stop layer between the electron-beam-evaporated Ti/Pt/Au/Ti Schottky gate electrode and the GaAs channel layer. In this structure, the gate metal/etch-stop layer Schottky contact is the key component, although these Schottky contacts are not intimate metal–semiconductor contacts, and are

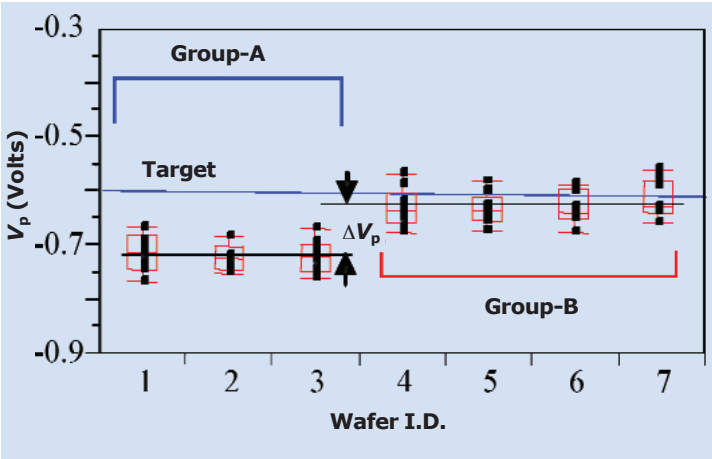

Figure 4: Pinch-off voltage versus wafer I.D. of a depletion-mode FET from a single fabrication run. Note that the ΔV_p of 100 mV between the two groups arises due to the difference in epitaxial layers.

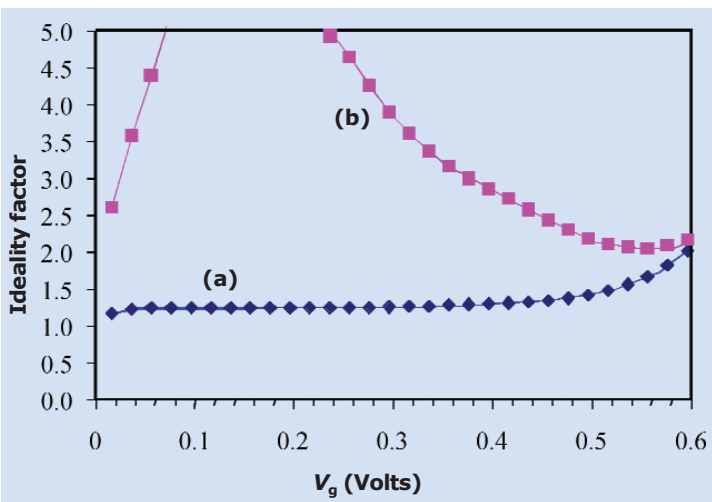

Figure 5: Ideality factor as a function of gate voltage of the Schottky contact. Curve (a) is generated from an FET with good electrical characteristics, and (b) from an FET with poor electrical characteristics.

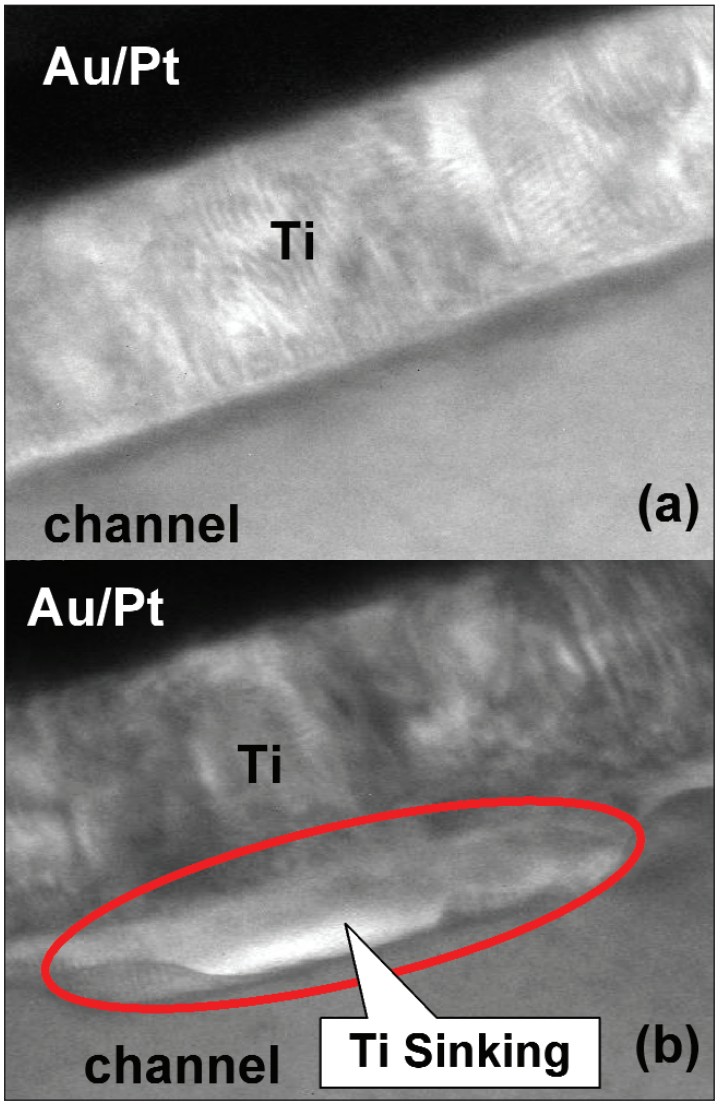

Figure 6: Transmission electron micrographs of the gate region. Image (a) is from the gate Schottky with n = 1.23 and image (b) is from the non-ideal Schottky contact with n > 2. Note the sinking gate, which is highlighted in (b).

separated by a thin inadvertent interfacial layer formed due to cross-diffusion, out-diffusion and chemical reactions between the metal and the semiconductor. It is therefore critical to optimize the gate definition process steps which prepare the surface consistently prior to gate metallization. Several wet and plasma surface passivation processes are investigated. The ideality factor, $n = (q/k_BT)\ (dV_{gs}/d\ln I_g)$, is determined from the forward I–V characteristics of the gate at 300K.

The change in ideality factor as a function of the applied voltage, as illustrated in Figure 5, is used to determine the quality of the metal–semiconductor contact. Curve (a) in Figure 5 is collected from an FET and fabricated with an optimized gate process. On the other hand, curve (b) in Figure 5 is collected from an FET with a pinch-off voltage of –0.2V and the saturation current was dropped by more than 10 times the target value. For an imperfect Schottky contact (Figure 5b), the ideality factor increases with bias to almost 5, and then decreases. Such a voltage dependence of n is very unique in III–V semiconductors with a high density of surface states. Surface imperfections and a sinking gate, leading to the distribution of interface states in the forbidden gap, are the major causes of non-ideal behavior in Schottky contacts, and are revealed by transmission electron microscopy (TEM) of the gate region, as shown in Figure 6.

Manufacturability

In addition to establishing the control procedures for the incoming epitaxial material, each process module in the fabrication steps was carefully optimized. The process capabilities (Cp, Cpk) were assessed from the electrical parameters of both HBT and FET devices, and the statistical data was used for circuit designs. Besides process control procedures, it is also critical

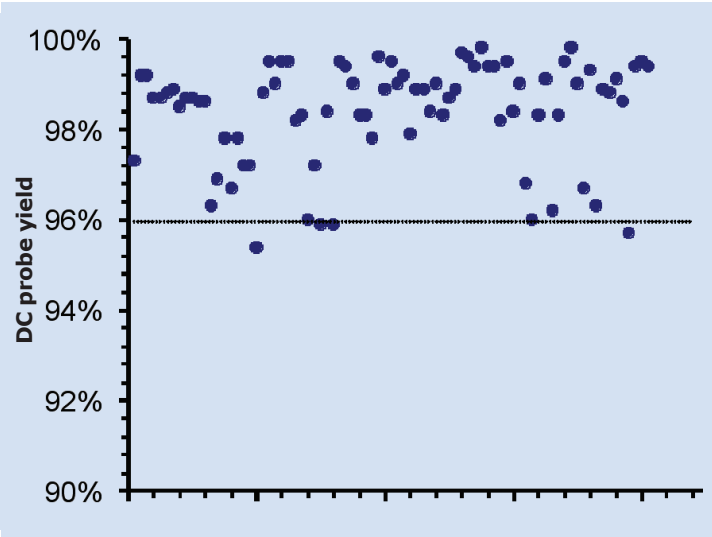

Figure 7: DC probe yield of BiFET designs as a function of wafer/lot numbers collected over a period of four months. Gross yielding dies per wafer is computed after performing a series of DC tests for both HBT and FET active devices as well as passive devices such as resistors and capacitors in the design.

that the FETs in the BiFET circuits can be probed, either directly or indirectly, in order to calculate the gross yielding dies per wafer accurately. For example, indirect measurement in the bias enable path could be simply toggling the gate voltage to the FET and measuring the bias voltage to the amplifier in the FET on-state and the bias leakage in the FET off-state. Extensive test coverage during the early stage in high-volume manufacturing will identify possible epitaxial material, process and/or tool issues. As a result, high DC probe yield in CDMA/WCDMA and WLAN products based on BiFET technology, comparable to HBT-only based products, have been achieved, and are depicted in Figure 7.

Summary

The importance of screening incoming epitaxial material has been shown to be crucial for achieving/maintaining high yield in manufacturing. To this end, the capacitance–voltage characterization method was used to qualify the FET-specific layers, along with the electrical characterization of HBTs using large-area processing in the BiFET wafers. The sensitivity of the C–V method was found to be adequate for quantifying growth run-to-run variations, and good correlation has been made to the FET electrical parameters at the end of the line. The bias-dependent ideality factor n and the decrease in transconductance g_m as a function of different process steps were studied, and optimized process conditions, which preserve the integrity of the FET and HBT, were chosen. With the implementation of stringent control procedures as well as circuit-validated control limits, high-probe yield in the BiFET-based circuits has been demonstrated. ■

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